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A SPREAD SPECTRUM COMMUNICATION TECHNIQUE

James Alfred Cocci

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THESIS

A SPREAD SPECTRUM COMMUNICATION TECHNIQUE

by

James Alfred Cocci

Thesis Advisor: Stephen Jauregui Jr.

September 1973

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A Spread Spectrum Communication Technique

by

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Submitted in partial fulfillment of the
requirements for the degree of

ELECTRICAL ENGINEER

from the

NAVAL POSTGRADUATE SCHOOL
September 1973

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ABSTRACT

A practical solution to the problem of realizing a signal processing method for a covert voice communications system was the objective of the thesis. Spread spectrum technology in the form of Golay complementary sequences implemented with acoustic surface wave devices was utilized to achieve this processing.

The resultant device was an audio transceiver MODEM in which a specially coded form of pulse code modulation (PCM) was applied to a voice signal to enable application of the spread spectrum concept. The technique exploited spread the 3 KHZ voice modulation over a one MHZ bandwidth. A method of PCM synchronization evolved which achieves system send/receive synchronization with a minimum of data loss and a minimum amount of actual hardware.

Highly involved theoretical analysis was de-emphasized in the thesis in order that engineering requirements could be satisfied in the working device that resulted.

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I. INTRODUCTION

Despite the degree of sophistication modern communications technology has attained, the problems of covertness and security still pose serious threats to military forces operating in hostile environments. The problem manifests itself in all scales of systems, whether it be large data communications networks, where long term sensitivity of the information may seriously affect national security, or in the simplest two-way radio link whose information is relevent only to a specific local application. The basic premise is that regardless of the apparent importance of any transmitted information, the use of this information by any hostile party could eventually be detrimental to the overall effectiveness of large scale operations.

To date, the method of denying enemy the use of our transmissions has been to cover the information through complex encryption schemes, thereby obscuring the information content of channels to other-than-intended users. This method is of course not to be undermined since some information retains its sensitivity for long periods of time and even an eventual compromise could have far reaching detrimental effects on items of highest national security. The encryption (and eventual decryption) process is realized by employing highly complex mathematical algorithms which code

the data to an appearance of arbitrary events and re-applying the algorithms to the encrypted signal to retrieve the original information content.

This of course necessitates the use of extremely complex hardware (and sometimes software) configurations which at times can be rather extensive in physical space consumption, cause undesired reliability problems and increase the cost of a system by a considerable amount. In the case of large scale communications systems, the security obtained may greatly outweigh these apparent disadvantages however, thereby fully justifying employment of such a scheme.

However, large systems are not the only types which may require some degree of security, since an application in which a small single channel circuit is utilized may have need for some type of cover also. When considering a small system, the tradeoffs considered above do not follow the same set of ground rules, since compactness and portability are usually prime criteria. Cost may also be a major factor. Certainly the full cover utilized in larger systems would be attractive in smaller units as well, but the complexity involved in the realization of such a scheme simply does not lend itself to efficient solution on a smaller scale. The main question that arises then is one of whether or not a small communications system can be provided with the ability to make difficult hostile access to transmitted information. The answer to this question lies in the field of technology known as Spread Spectrum Transmission Methods.

A. STATEMENT OF THE PROBLEM

Many present United States military operations are coordinated by means of voice transceiver networks which vary in complexity from simple single-channel to multiple-subscriber several-channel systems.

The information carried on these networks may be seemingly unimportant to individual users, but the collection of transmissions on any one system may well lead to the compromise of a significant overall operation. It is evident that since the operation of a network of this type is extremely simple, any intelligence effort conducted by a hostile force is very likely to give this force access to any or all of the information needed to surmise the nature of the military operation being surveyed.

The necessity of making difficult hostile access to this information was the driving force for this thesis.

B. DEFINING THE THESIS

The initial consideration was that of defining what type of security would be best suited to the application at hand. Communications Security, as defined by today's usage, implies the employment of highly complex encryption/decryption schemes which ensure the long term security of transmitted information. However, if one considers the nature of the information transmitted on these voice networks, it is easily surmised that this data is extremely perishable, since within a few hours of disclosure, the missions controlled by the operation are completed, thus rendering the information

useless to any hostile forces. This indicates that a lesser degree of security would provide the necessary denial capability, and a simple premise could then be invoked at this point: If the enemy did not know the fact that you were transmitting, he would then be unable to inercept your transmission and therefore would be denied the information carried in that transmission. With this hypothesis accepted, the problem falls into the realm of transmission security, or covert communications, and the problem can be concisely stated: "Devise a scheme that will integrate the element of covertness into a small scale audio transceiver network."

1. General Considerations

The general nature of the problem statement presented a wide range of selections for the specific thesis application. The main question that arose was "What type of product and how much of this product would be necessary to satisfy the requirements imposed?" Development and presentation of a purely theoretical solution to the problem was considered, but the value of such an approach was deemed unsatisfactory since it would not actually solve the problem at all, but instead would advance the problem solution no further than its original status.

To the other extreme, fabrication of an entire working finished product would also have adverse effects. The circuitry required to realize such a system would have included devices which would have little or no bearing on the actual problem solution (the covertness) since amplifiers,

transmitters and receivers and associated antennas would be required. Design and construction of these components would have demanded a significant amount of effort which would tend to obscure the importance of the actual coding and hardware required to accomplish the covertness and thus detract from the area where all of the concentration was required.

The approach decided on then was to design and fabricate a working model which would completely realize the theory involved, while at the same time would represent neither a purely theoretical research effort nor a finely detailed working system. As previously mentioned, the most likely candidates for omission were the transmit and receive stages, or RF stages, and various stages of amplifiers. With this in mind the problem then degenerated to one of design and construction of a voice modulator-demodulator (MODEM) unit with an IF output/input which incorporates the necessary hardware to provide a capability of covertness for eventual transmission.

2. Physical Considerations

Since the eventual circuitry would have to be incorporated into the same operational medium as the present network, the first set of criteria considered was that of compactness, reliability, cost and simplicity. Compactness indicated that the use of integrated circuitry (IC) would be required, and specifically the use of standard "off-the-shelf" integrated circuits would enhance reliability and minimize the cost. Simplicity would then follow as a natural

result since integrated circuits allow the system to be designed in functional modules, as opposed to integrating many discrete components.

3. Theoretical Considerations

To realize a covert transmission network it was evident that some type of signal processing would have to be employed that would spread the spectrum of the baseband signal and thus allow the same total energy to be transmitted at a lower amplitude and be buried in the surrounding noise level. The ability to extract this signal from within the noise implied that a significant amount of signal processing would be required at the receiver as well. This processing was then the next logical consideration.

Since the transmitted signal was to be dealt with in a relatively noisy medium, all stages of processing had to be relatively immune to noise interaction. It was decided that the audio signal would first be digitized, and processing could commence at that point. The first stage of processing was to be the modulation of the digitized signal.

There are several types of pulse modulation in use today, a partial list of which includes pulse amplitude modulation (PAM), pulse position modulation (PPM), pulse width modulation (PWM) and pulse code modulation (PCM). If one considers the first three of these however, it can be seen that the information is dependent upon actual pulse characteristics, which could be seriously affected when the signal lies within the noise levels. PCM however uses only

the presence or absence of pulses to convey information, thus giving the greatest degree of noise immunity over the other modulation types. It was therefore decided that pulse code modulation would be the first stage of the overall signal processing scheme for this application.

Representation of the binary states was the next item of consideration. Since it was previously stipulated that the eventual product would be kept as simple as possible, on-off keying (OOK), which implies the presence of energy to represent the "on" state and the absence of energy for the "off" state, was the most obvious choice.

In order to allow the transmitted signal to be extracted from the noise by an intended receiver, it was necessary to employ a processing scheme that would coherently disperse the PCM signal energy such that the signal processing gain in the retrieval process would be large enough to force the buried signal to within detectable proportions. Representation of each of the PCM pulses by a predetermined binary sequence, coupled with matched filtering at the receiver was the preliminary choice, since the PCM form the signal would be completely compatible with digital processing methods. This choice had to be further refined however since different lengths and types of codes yield quite different results in the autocorrelation process. Further consideration then generated the additional requirements of high noise immunity, low probability of error (ambiguity) and non-interference in the case of code overlap caused by a

sufficiently high data rate. All of these requirements led to the employment of a coding scheme that until now had not been used in a practical communications system - Golay Complementary Sequences. It was further decided that this coding would be realized through the use of acoustic surface wave devices.

Having specified the type of signal processing to be employed in the finished product, the scope of the thesis had thus been defined. The next step was to design and fabricate the hardware required to realize the concept, the process of which is described in part III of this thesis. However, in order to acquaint the reader with Golay complementary sequences and acoustic surface wave devices, part II of the thesis provides a brief but pertinent introduction to both of these topics.

II. REALIZATION OF THE CODING SCHEME

This section provides the reader with sufficient background on surface wave devices and Golay sequences to be able to follow the design and fabrication of the MODEM hardware. No attempt is made here to present the theoretical concepts involved with these two subjects. For a more complete presentation of surface wave devices and their applications, Refs. 1 - 5 should be consulted. Similarly, Refs. 6 and 7 provide a more complete background on Golay complementary sequences.

A. ACOUSTIC SURFACE WAVE DEVICES

Acoustic surface wave devices (ASWD) operate on the principal that a physical wave will propagate on the surface of an elastic solid, a principal investigated by Lord Rayleigh in the nineteenth century, and accordingly these waves have come to be known as "Rayleigh Waves". More specifically, these surface waves propagate at a velocity 10^5 slower than that of free space electromagnetic waves, independent of frequency, which implies that the surface wavelength will be scaled down by the same factor.

It was discovered that in the case of a piezoelectric solid, these waves could be excited electrically, and conversely the physical wave could be re-converted to electrical energy. These basic concepts are best illustrated by example.

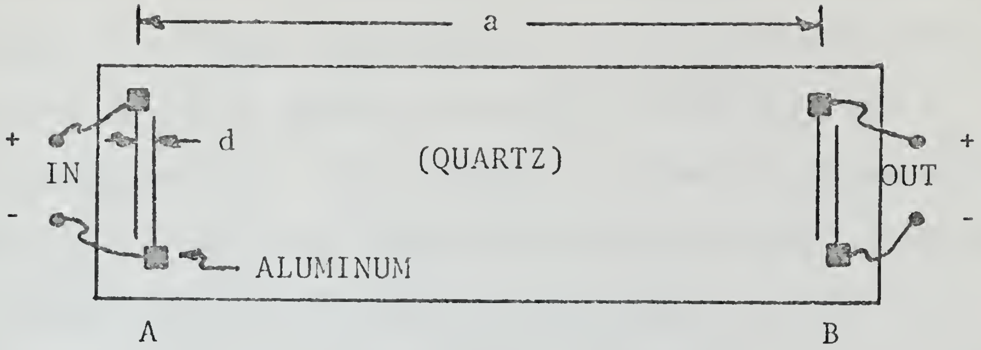

FIGURE 1

ELEMENTARY SURFACE WAVE DEVICE

Figure 1 depicts a piezoelectric crystal, such as quartz, upon which has been deposited aluminum fingers, or transducers. For example purposes, consider the dimensions shown to be as follows: d equals 0.03 millimeters and a equals 45.0 millimeters. If transducer A is excited by an electrical impulse the convolution process of this impulse with the transducer will result in the launching of one sinusoidal cycle on the substrate surface. The dimension d is equal to one-half of the surface wavelength so the overall wavelength is 0.06 millimeters. This wave will propagate at a velocity of 3 x 10^3 meters per second (10^5 slower than free space velocity) and will therefore arrive at transducer B 15 microseconds later. The energy in the physical wave will then be coupled out of the device by transducer B and one cycle of electrical energy will be present at the output. Since the surface wavelength was 0.06 millimeters, applying the 10^5 conversion factor yields a free space wavelength of 6 meters, or a frequency of 50 megahertz. This simple

example serves only to illustrate the properties mentioned previously, but simple architectural modifications to the transducers could be applied to modify the device for a specific application. As an example, assume it is desired to generate a phase coded sequence of four sinusoidal pulses. It is further stipulated that the individual pulses are to contain four cycles of 50 megahertz frequency, and the relative phases of the sequence pulses are + + + -. A surface wave device that will accomplish this is shown in Figure 2.

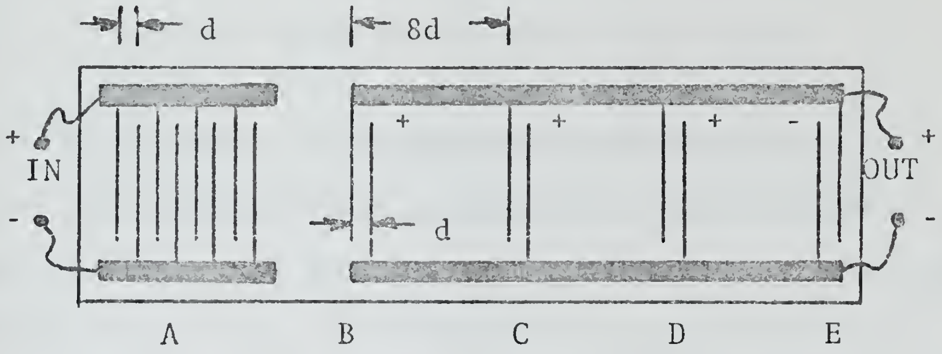

FIGURE 2

PHASE CODING ON A SURFACE WAVE DEVICE

Transducer A, the launch transducer, is composed of four finger pairs so that if an impulse is applied at the input, four sinusoidal cycles will be launched on the substrate surface. Close inspection of the four receive transducers shows that the phase coding is implemented by the relative positions of the finger pairs. Transducers B, C and D are in phase with A, whereas transducer E is 180 degrees out of phase with A. Therefore the waveform that is coupled out of

the device by the set of receiver transducers is as depicted in Figure 3. This waveform exhibits the desired properties,

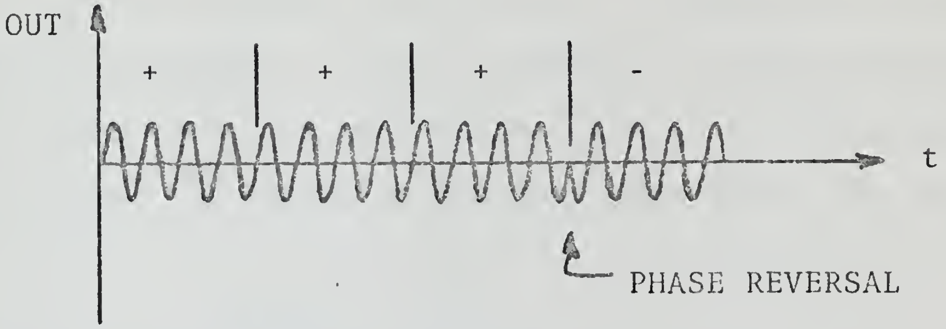

FIGURE 3

IMPULSE RESPONSE OF ASWD OF FIGURE 2

that is the relative phases of the pulses are + + + -.

The following section extends this application of ASWD's to show how they may be used as matched filters for Golay sequences.

B. GOLAY COMPLEMENTARY SEQUENCES

Concisely stated, Golay complementary sequences are those binary codes which have an infinite correlation peak to peak ambiguity ratio when detected with a matched filter. As previously stated, no theory is to be presented as a part of this thesis concerning these codes and appropriate references were made. Instead, a simple example illustrating this unique property will best suit the purposes of the reader for this application. Suppose it is given that the binary sequences 1 1 1 0 and 1 1 0 1 are in fact Golay complements. These sequences could be represented by phase coded waveforms as

cited in the previous example by assigning to two separate pulse trains, A and B, the relative phases + + + - and + + - + respectively. The two sequences could be generated by two distinct surface wave devices. To generate the autocorrelation functions of these sequences, a minor modification to the devices must be made in the form of an added transducer as shown in Figure 4. Assuming one device for each of the codes, the process would be as follows. If both ASWD's were excited by the same impulse, applied at port X, then the two waveforms coupled out from port Y would be of equal length and would be phase coherent. A matched filter technique would then be used to generate the autocorrelation functions. Consider the case of code A. If the bi-phase representation of this code was fed to port Y of its matched ASWD, then the autocorrelation function R_{AA} would appear at port Z. Tabular computation of R_{AA} is given in Table 1.

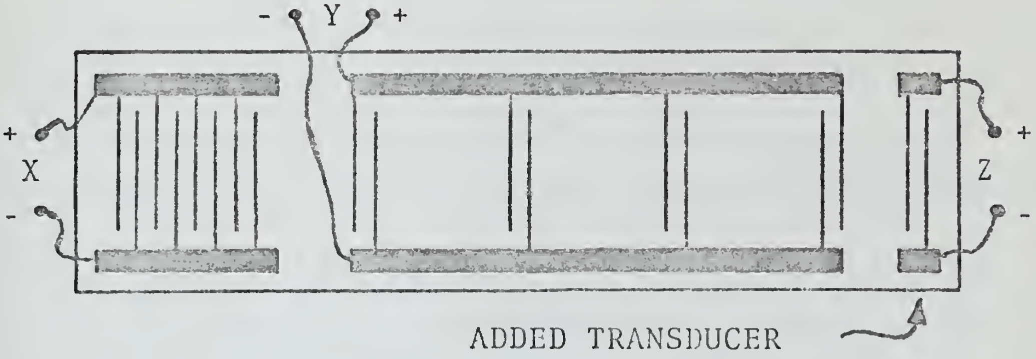

FIGURE 4

ASWD MODIFICATION FOR CORRELATION PROCESS

TIME	A*A	R_{AA}
1	+++- +++-	-1
2	+++- +++-	-1 0
3	+++- +++-	-1 0 1
4	+++- +++-	-1 0 1 4
5	+++- +++-	-1 0 1 4 1
6	+++- +++-	-1 0 1 4 1 0
7	+++- +++-	-1 0 1 4 1 0 -1

TABLE 1

COMPUTATION OF R_{AA}

The sequence -1 0 1 4 1 0 -1 represents the relative phases and amplitudes of the pulses comprising the function R_{AA}. Similar analysis for code B would yield R_{BB} equal to 1 0 -1 4 -1 0 1. The property of the Golay codes is such that the algebraic sum of the autocorrelation functions must be obtained to produce the resultant correlation function. This function is shown in Figure 5. The resultant correlation sequence is then 0 0 0 8 0 0 0, which exhibits the property of an infinite major peak to sidelobe peak ratio, in addition to a 3 DB major peak gain over the single code case. Since this is the best theoretically obtainable correlation result (least probability of ambiguity between the major

peak and sidelobe peaks), then it was hypothesized that in

R_{AA}:	-1	0	1	4	1	0	-1
R_{BB}:	1	0	-1	4	-1	0	1
$R_{AA} + R_{BB}$:	0	0	0	8	0	0	0

FIGURE 5

SUMMING R_{AA} AND R_{BB} TO OBTAIN THE CORRELATION

practice it would also be the best result.

The increased processing gain (conventional codes would yield a final correlation peak of amplitude 4 with the addition of existing sidelobes) implied that in a noisy environment this coding scheme would work best. Furthermore, it can be shown that in the case of code overlap, that is the case where codes A and B are transmitted periodically such that the individual codes overlap, the resultant correlation process will yield a unique set of correlation peaks with no sidelobe interference. This phenomenon is demonstrated in the MODEM operation description in part IV of this report. Golay complementary sequences were therefore chosen for use in the resultant MODEM.

C. ACTUAL MODEM CODING SCHEME

The actual Golay sequences used in the MODEM are of length sixteen and are shown in Figure 6. Based on the previous analysis, it can be seen that in the normalized case the individual autocorrelation functions will have major

CODE A: 1 1 1 0 1 1 0 1 1 1 1 0 0 0 1 0

CODE B: 0 1 0 0 0 1 1 1 0 1 0 0 1 0 0 0

FIGURE 6

GOLAY SEQUENCES OF LENGTH SIXTEEN

peaks of amplitude 16, and the sum of these will yield a peak of amplitude 32 with complete sidelobe cancellation.

These codes were in fact implemented on acoustic surface wave devices employing a special architectural layout of the transducers. A photograph of one of the devices is shown in Figure 7.

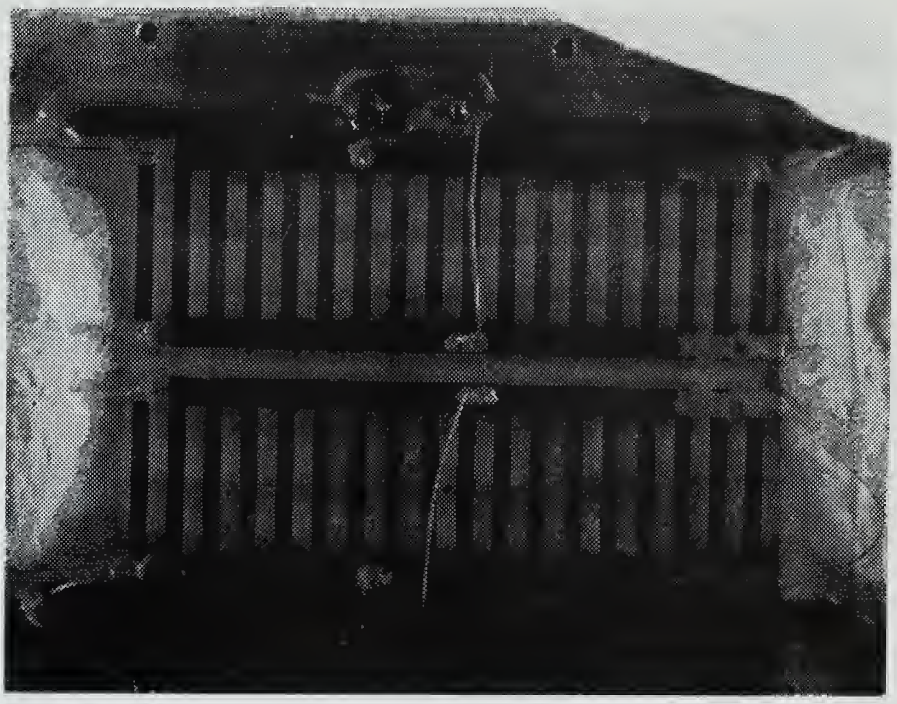

FIGURE 7

ACOUSTIC SURFACE WAVE DEVICE (MOUNTED)

On a single quartz substrate were deposited two devices, one each for code A and code B respectively, giving the effect of a single device generating both of the sequences simultaneously. In the photograph it can be seen that there are single transducers at both ends and sixteen bi-phase coded transducers in the center. Each transducer consists of ten finger pairs spaced such that the center frequency of the devices is 21.4 megahertz.

For a detailed description of the Golay sequences and the ASWD's, including physical characteristics, impulse response and autocorrelation processes, the reader is referred to Appendix A of this report.

III. SYSTEM DESIGN AND FABRICATION

System design and fabrication was predicated on the criteria previously mentioned. That is, it is to be a working model which employs the acoustic surface wave devices and Golay sequences to illustrate how an audio signal may be dispersed in such a manner that in a transmitted form the signal would be below the inherent noise level, and at the same time an intended user could compress the signal and retrieve the information content in the simplest way possible. Since the MODEM was to be illustrative of the involved principals, the necessity of a functional breakdown of specific circuit functions was needed. That is, the functions of modulation, dispersion, encoding, decoding and compression, and demodulation would have to be physically separate in order to present a clear picture of the entire signal processing scheme. This provided the guidelines for the eventual packaging of the final product. The first step however was that of deciding what these actual functions would be.

A. OVERALL SYSTEM DESCRIPTION

Figure 8 depicts a general block diagram of what a complete transceiver would consist of. Basically, the audio signal is processed into a form suitable for transmission, fed to the transmitter stage in this form and accordingly is sent out over the air at a level such that at the receiver

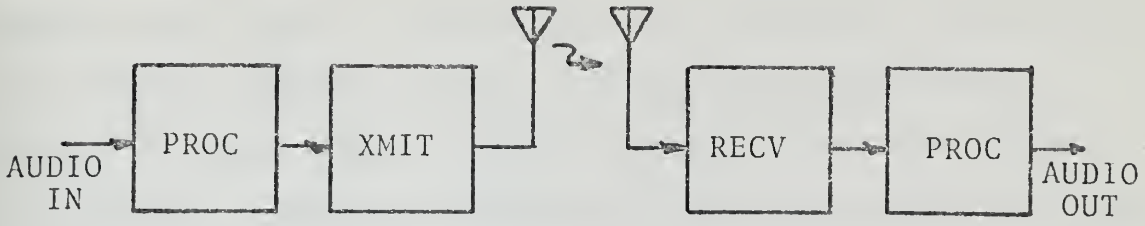

FIGURE 8

COMPLETE SYSTEM BLOCK DIAGRAM

the signal is buried in the noise. At the receiver the proper frequency band is received and fed to the inverse processing hardware, which extracts the signal from the noise and processes it back to an audio output.

Since the major concern of this thesis was the processing of the signal into and out of a dispersed format, it was decided to eliminate the transmit and receive RF stages and therefore channel all of the effort to the signal processing aspects. The general block diagram then took the form shown in Figure 9.

Using this representation as a starting point, the first task was to decide on the physical format of the finished product. Some considerations involved in this process were

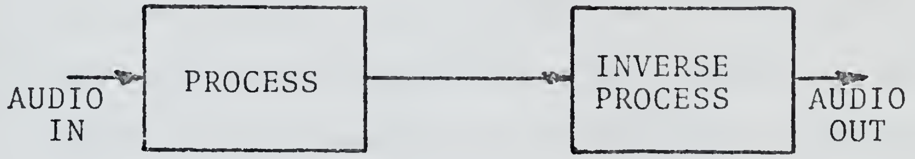

FIGURE 9

MODIFIED GENERAL BLOCK DIAGRAM

(1) the device was to be as self-contained as possible. This feature would greatly simplify set-up procedures and provide for a cleaner looking set-up. (2) The major functions involved in the various stages of signal processing should be physically segregated in order to make more effective the presentation of the device. This would ease the understanding of the principals involved since a signal could be logically traced through all stages of processing. The format decided on then was as shown in Figure 10.

At the transmit side an audio signal would be fed to a unit that would pre-process the signal into a modulated format, the output of which would basically be a pulse code modulation representation. This signal would then go through an interface unit, which would transform it to a form compatible with a dispersive device, which would apply the Golay coding to the signal. At the receive side the incoming signal would be compressed, thereby simulating the extraction from noise, and an interface unit would then make this representation compatible with the demodulation unit. This unit would convert the reconstructed PCM signal back to an audio form. An additional desired function was that of providing power to the individual active units, so the decision was made to fabricate a self-contained power supply as well. The only function that would rely on external components would be that of amplification of the signal in its RF format, which would be accomplished through the use of laboratory type amplifiers.

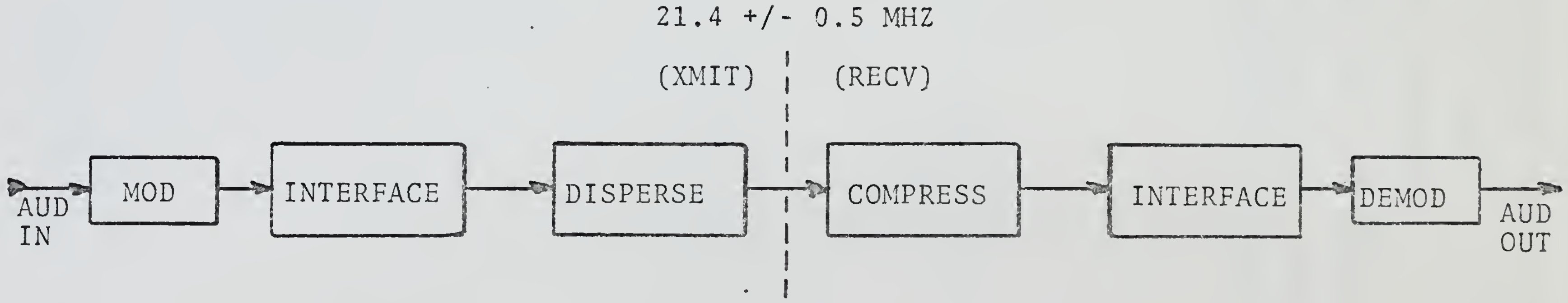

FIGURE 10

SYSTEM FUNCTIONAL REPRESENTATION

This functional breakdown provided for a more logical design and fabrication process, as the system could be designed and built from the "outside-in". This evolution process is shown in Figure 11.

In its final form, the system was constructed and packaged as shown in Figure 12. Description of the individual functions is provided in the following sections.

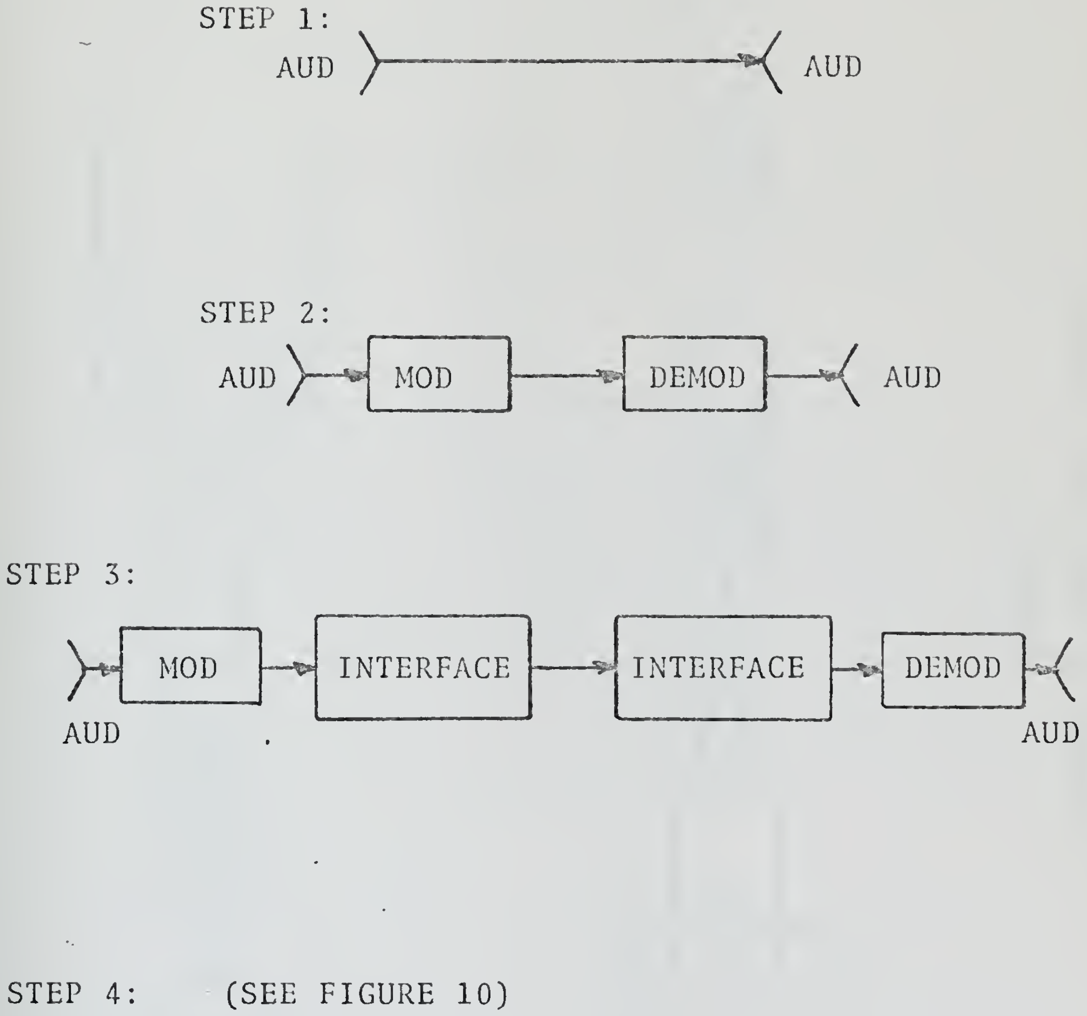

FIGURE 11

SYSTEM EVOLUTION PROCESS

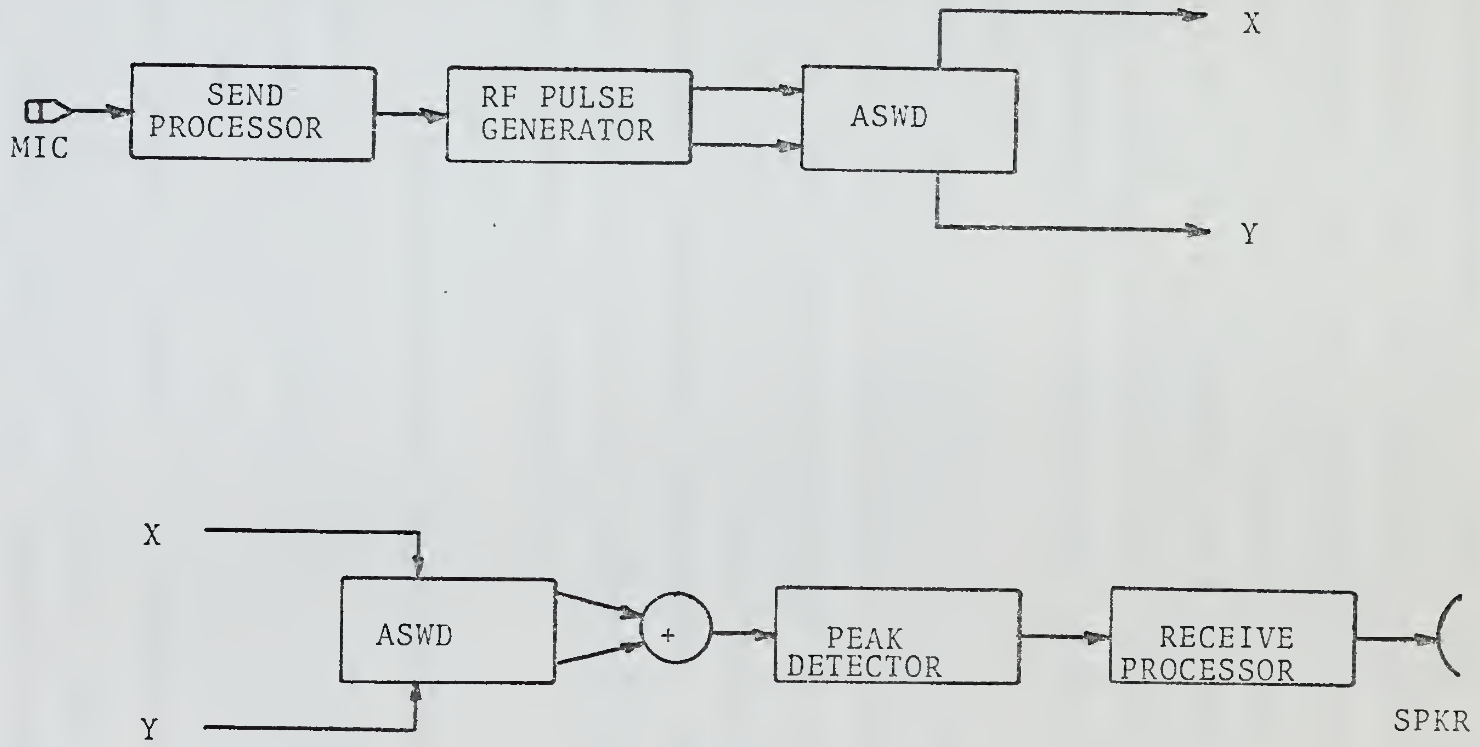

FIGURE 12

COMPLETED SYSTEM BLOCK DIAGRAM

B. THE MODULATION SCHEME

The modulation and eventual demodulation of the audio signal is accomplished by the units labelled SEND PROCESSOR and RECEIVE PROCESSOR respectively. The requirements imposed on these units were (1) conversion of the audio signal to a digital form, (2) pulse code modulation of this digital signal, (3) formatting the PCM signal such that timing synchronization could be achieved, (4) demodulation of the PCM signal, including extraction of the timing information and (5) conversion of the reconstructed digital signal back to an audio form.

Item (3) above evolved into one of the more significant aspects of the thesis and resulted in the docketing of a patent disclosure [Ref. 8] on the timing concepts that were developed. For purposes of readability however, only the actual signal format will be presented in the thesis body, and the theory involved in the synchronization concept is outlined in detail in Appendix B.

1. Send Processor

A block diagram of the send processor is depicted in Figure 13. The circuit consists of an audio preamplifier which amplifies the incoming signal to the full scale range of the next component, the analog-to-digital (A/D) converter. The audio signal is sampled at a predetermined rate, which is determined by the timing hardware. This rate is adjustable, but due to timing limits imposed by the A/D converter, this rate is nominally set at approximately 15 kilohertz.

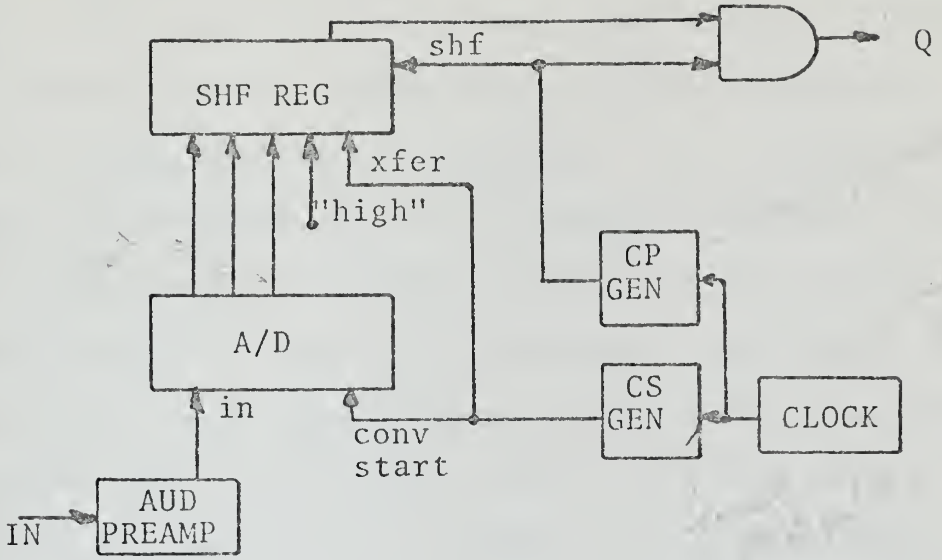

FIGURE 13

SEND PROCESSOR BLOCK DIAGRAM

The signal is quantized to eight levels in the digitizing process, resulting in a 3-bit binary representation of each sample. These three bits are fed to a parallel-to-serial shift register, which the timing hardware uses to manipulate the data into the PCM format. The timing waveforms are as shown in Figure 14.

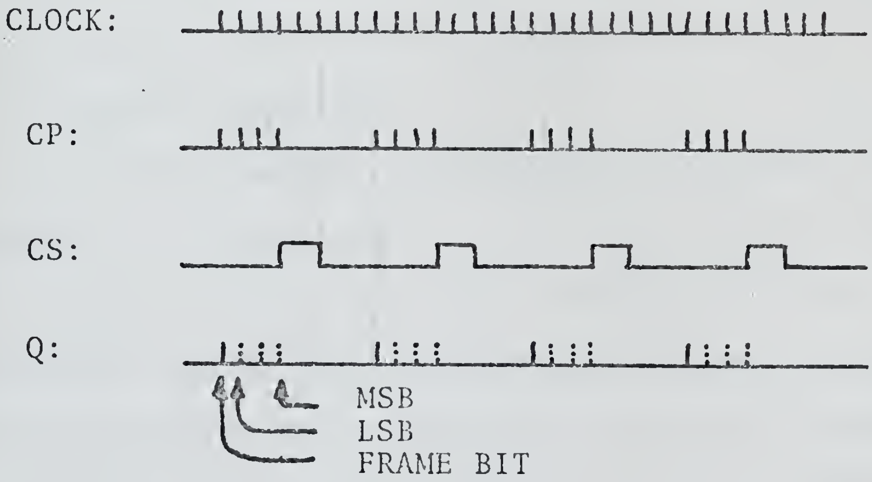

FIGURE 14

SEND PROCESSOR TIMING WAVEFORMS

A digital oscillator produces the master timing pulses (CLOCK), which are modified by logic circuitry to produce the actual timing signals used in the circuit. The pulse CS serves to accomplish three functions: (1) its leading edge triggers the sampling process in the A/D converter, (2) the "high" state serves to disable parallel entry of data into the shift register during the conversion process and (3) the trailing edge causes the newly converted data to be entered in parallel into the register. The shift register is clocked by the waveform CP, so that the shifting operation occurs only during the first four clock intervals of each 8-bit frame. Note that the first bit of the shift register is hard-wired to a "high" level. This will generate the "frame bit" of each frame, and the resultant output data stream will be as shown in waveform Q. This format is such that the first bit of each frame is the frame bit, followed by the three bits of data, which in turn are followed by four blank clock pulse intervals. The format of the outgoing signal therefore adheres to the requirements of the synchronization concept described in Appendix B.

2. Receive Processor

A block diagram of the receive processor is shown in Figure 15. This circuit consists of a phase locked loop which is used to lock on to the incoming frame bits and generate the timing for the remainder of the circuit. A serial-to-parallel shift register accepts the incoming data stream and has its parallel outputs tied to a buffer register,

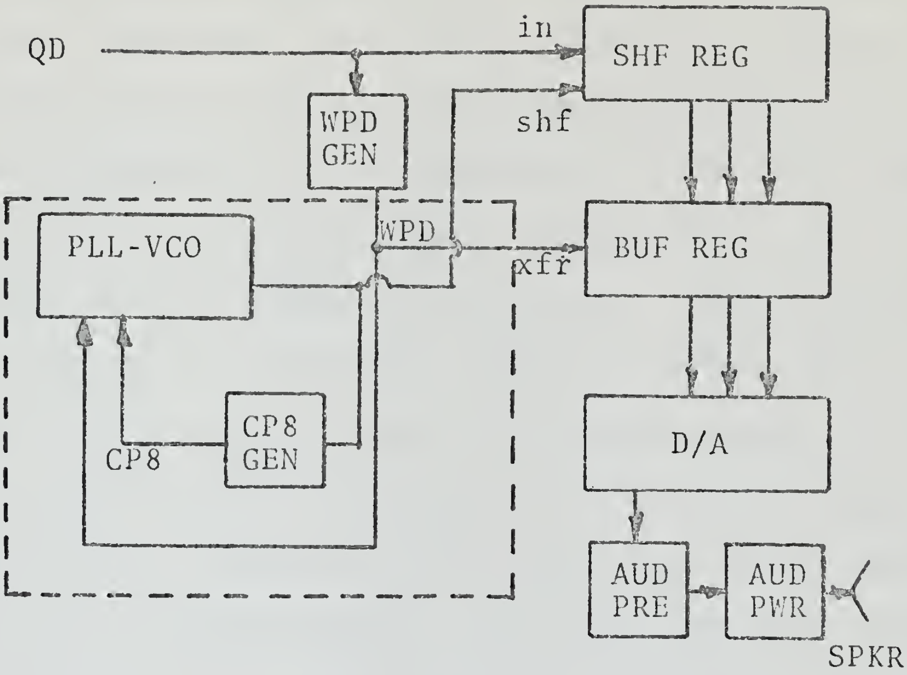

FIGURE 15

RECEIVE PROCESSOR BLOCK DIAGRAM

which is used to hold the 3-bit samples for the digital-to-analog (D/A) conversion process. The output of the D/A converter is then fed to an audio preamplifier and power amplifier to produce the desired output. The associated timing waveforms are shown in Figure 16.

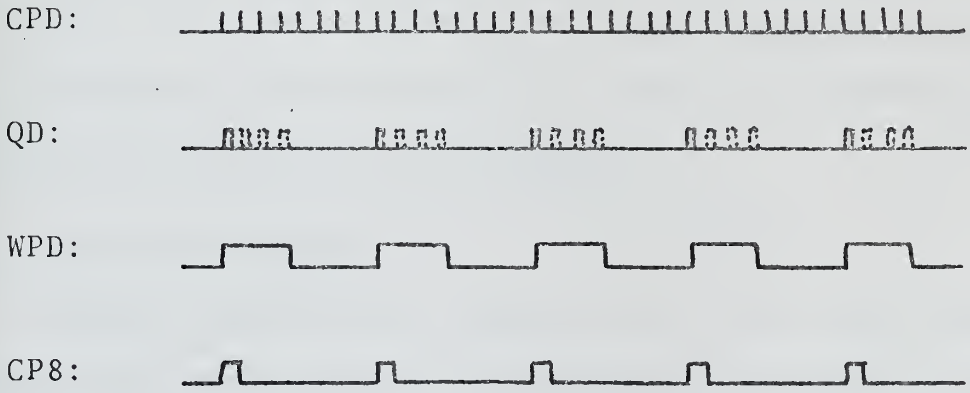

FIGURE 16

RECEIVE PROCESSOR TIMING WAVEFORMS

The voltage controlled oscillator (VCO) in the phase locked loop generates the receiver master clock pulses (CPD) which are used to clock the input shift register. As described in Appendix B, this waveform is locked onto the frequency of the incoming signal, so the data will in fact be shifted end-off through the register. The incoming data is also fed to the word pulse generator (WPD), which is used to serve two functions. First, the leading edge of this pulse is used by the PLL to phase lock on every eighth pulse of CPD, which is depicted by CP8, and thus ensure send-receive clock synchronization. The trailing edge of WPD is used to perform the parallel entry of data into the buffer register which, as outlined in Appendix B, will occur when the proper data frames reside in the shift register. Therefore the proper data bits are converted back to analog form and will appear at the output of this unit as a voice signal.

All of the integrated circuits used in the fabrication of the send and receive processors were standard off-the-shelf type, which was in keeping with the original set of criteria. The exact details of these units, including wiring diagrams, description of IC's used and individual IC functions are presented in Appendix C.

C. INTERFACE ELEMENTS

Having completed the fabrication of the send and receive processors, the status of the MODEM had advanced to Step 2 of the evolution process shown in Figure 11. The next logical design step was that designing the elements necessary

to interface the PCM signal with the acoustic surface wave devices.

Since each pulse of the data stream was to be used to drive the ASWD's, it was necessary to experimentally determine what type of driving function should be used for this purpose. Up to this point only electrical impulses had been used for this process, but it was discovered that the amount of energy this method supplied to the devices was insufficient to warrant usage in a practical application. Instead, a pulse of RF energy whose width was kept in the range 0.5 to 1.1 microseconds and whose carrier frequency was close to that of the center frequency of the devices produced resultant correlation peaks that were greater in amplitude and of the same resolution as those in the impulse case. It was therefore decided to use this type of driving function to excite the ASWD's.

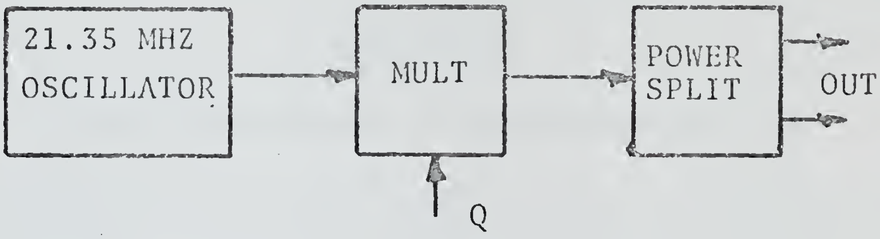

FIGURE 17

RF PULSE GENERATOR BLOCK DIAGRAM

1. RF Pulse Generator

The resultant send-side interface unit, the RF pulse generator, is shown in block diagram form in Figure 17. The circuit employs a free-running crystal controlled oscillator

whose output frequency is 21.35 megahertz, fed to one input of a multiplier circuit. The other input to the multiplier is driven by the data stream created by the send processor, labelled Q. This process has the effect of gating the RF energy "on" during the occurance of a data pulse and gating it "off" when no pulse is present, which is shown in Figure 18. Therefore the pulse width is controlled by the width of the pulses in the pulse train Q. This pulsed RF is then fed to a power splitter to provide two identical outputs, which as the reader may recall is necessary since two ASWD's (the Golay complements) must be driven simultaneously.

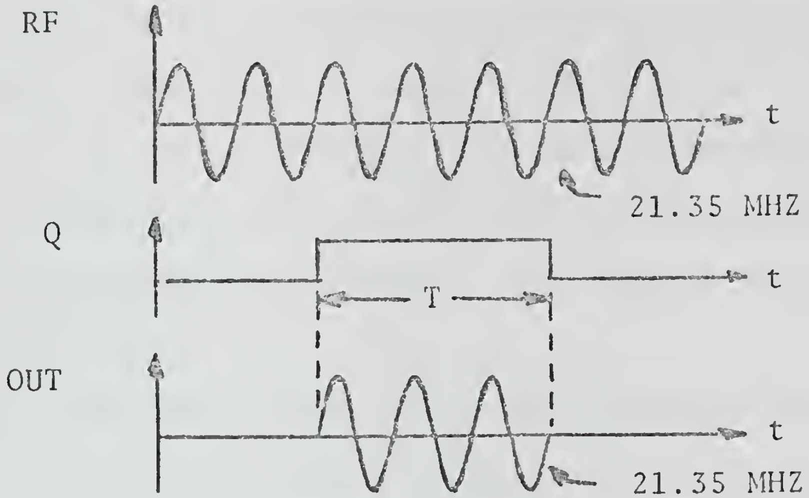

FIGURE 18

VOLTAGE WAVEFORMS OF RF PULSE GENERATOR

2. RF Peak Detector

At the receive side of the MODEM, it was required to interface the correlation peaks of the ASWD's to the input of the receive processor. This is the function performed by

the RF peak detector, which is shown in block diagram form in Figure 19. Figure 20 depicts the waveforms associated with the various stages of this circuit.

The correlation peaks from the ASWD's are fed through a simple diode detector which extracts the envelope from the peaks. This waveform is then fed to a variable threshhold comparator which outputs a pulse of fixed width and amplitude whenever the input crosses the reference level voltage. This pulse is then used to trigger a monostable multivibrator whose output signal (QD) is compatible with the receive processor circuitry. The pulse width of this signal is a variable parameter, to allow for slight instabilities in the timing synchronization hardware. The receive-side interface is thus achieved.

The evolution process had thus progressed to Step 3 of Figure 11, leaving only the addition of the acoustic surface wave devices to complete the MODEM fabrication process. For a detailed presentation of the interface elements, the reader is referred to Appendix D of this report.

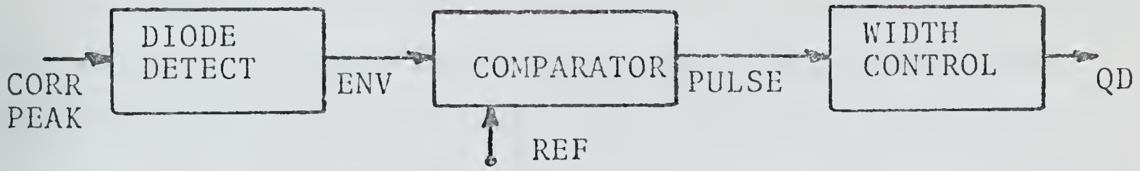

FIGURE 19

RF PEAK DETECTOR BLOCK DIAGRAM

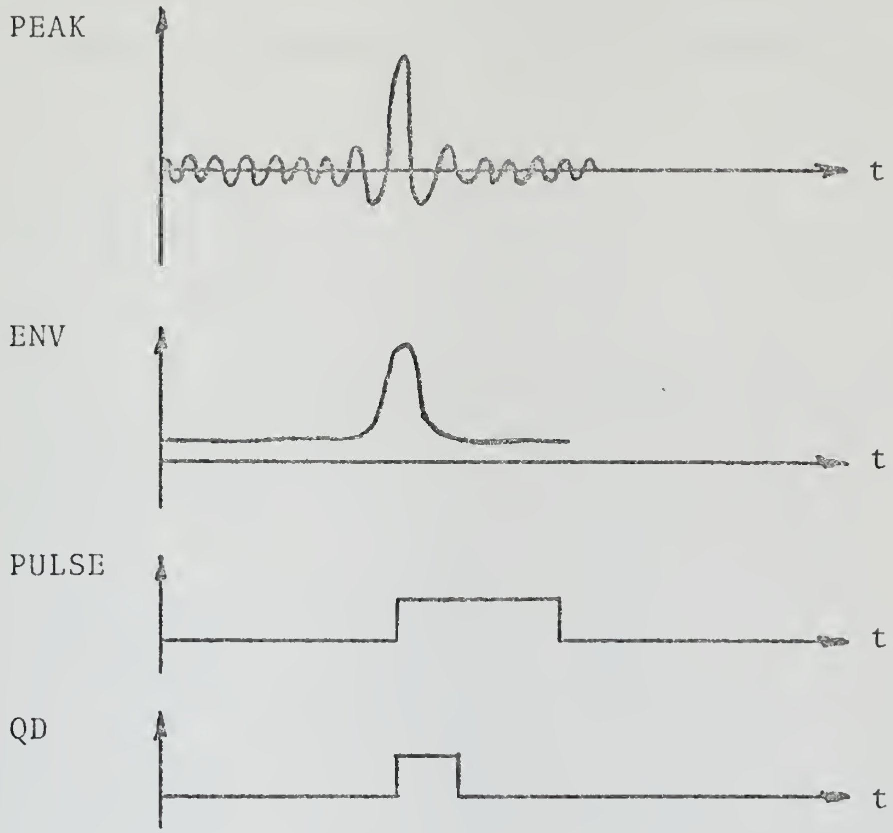

FIGURE 20

RF PEAK DETECTOR WAVEFORMS

D. THE COMPLETED SYSTEM

To complete the MODEM fabrication, the acoustic surface wave device, RF amplifiers, microphone and speaker were then included. Also, a self-contained power supply was fabricated and included as part of the overall system which is shown in Figure 21. As previously stated, the MODEM was built in functional modules, so the componenets of the physical device match one-for-one the blocks shown in Figure 21.

Appendix E contains a detailed description of the power supply wiring, as well as the physical details on the MODEM, such as cabling and external test point connections.

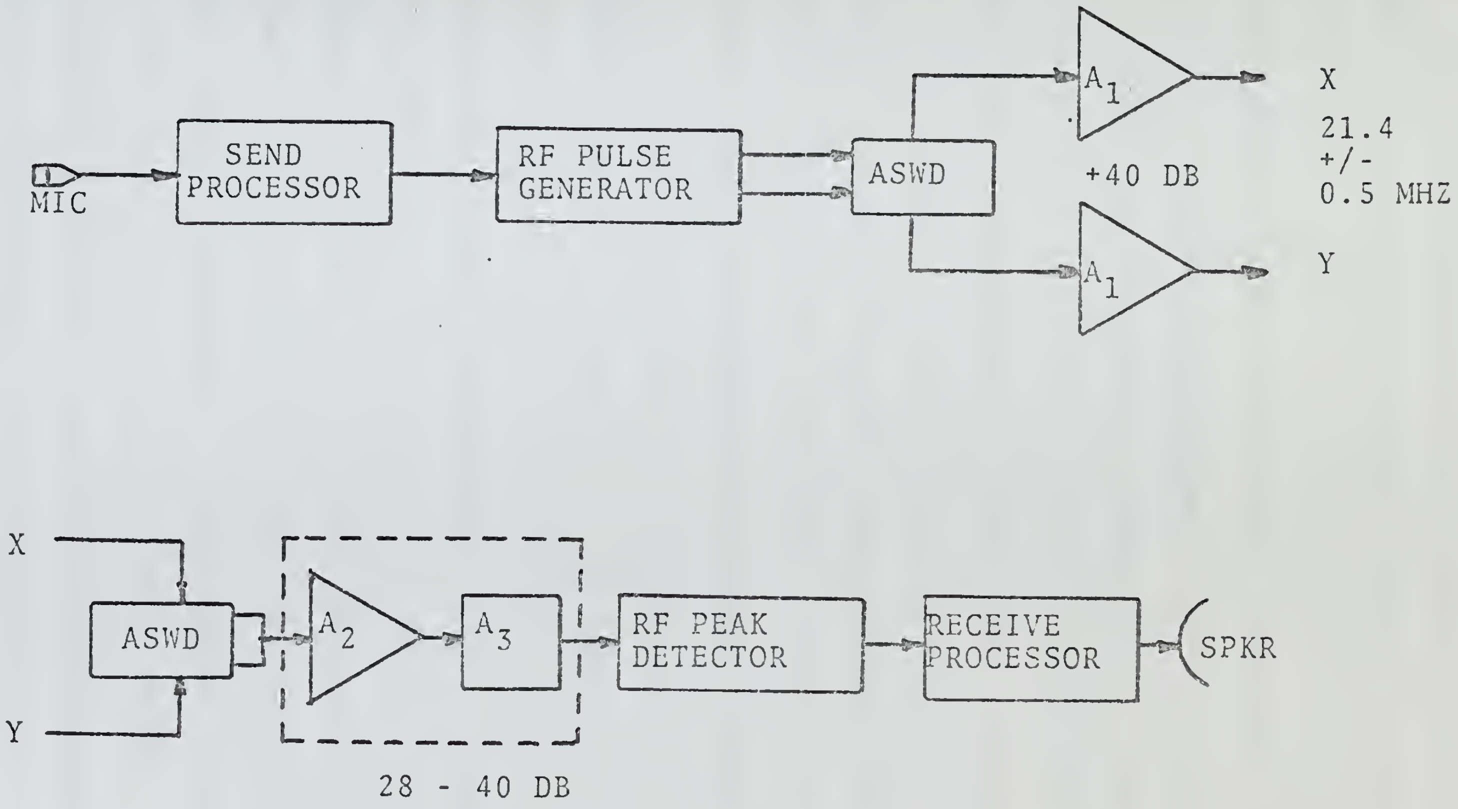

FIGURE 21

COMPLETED MODEM

IV. MODEM OPERATION

The most effective way to describe the operation of the MODEM is to trace the various stages of signal transformation through the circuitry. This section illustrates all of the signal representations and timing waveforms throughout the system by means of photographs, which are shown in Figures 22 through 34. Instead of referring to these photographs by figure number, the following narrative traces the signal in the order corresponding to the figure sequence.

In the send processor the master clock is running at a frequency of 125 kilohertz, thereby producing a continuous stream of timing pulses (CLOCK). This pulse train is modified by logic circuitry to produce the actual timing waveform (CP) used in the processor. An incoming audio signal is sampled upon the occurance of the convert start (CS) pulse and the 3-bit result is stored in a shift register. CP is then used to clock the register, thereby producing the formatted PCM output illustrated by Q. The sample in this example is a binary 1 1 0, which corresponds to a half scale value at the A/D input (the bits are arranged in reverse order, least significant to most significant in the frame).

In the RF pulse generator, an oscillator is generating a continuous sinusoidal waveform of 21.35 megahertz frequency which is modulated by Q and split to produce two output

streams of pulsed RF (RF PULSES). The width of these pulses is variable, and is equal to the pulse width of Q.

The pulsed RF is then used to excite the acoustic surface wave devices, the outputs of which are depicted by ASWDA and ASWDB. It is of interest to note that these responses differ radically from the impulse responses shown in Appendix A. Also note that the 16 microsecond long ASWD responses overlap, since the data rate is 125 kilohertz.

These responses are then amplified and fed to the respective matched ASWD's, which produce the autocorrelation functions R_{AA} and R_{BB}. Inspection of these functions reveals that even though the actual coded waveforms generated by the dispersive device are quite different from the impulse driven case, the autocorrelation functions are in fact the same as in the impulse situation in Appendix A.

These functions are then summed to produce the resultant correlation peaks ($R_{AA} + R_{BB}$), which are then envelope detected, as depicted by ENV. Note that even though the output of the dispersive devices exhibited an overlap condition, no sidelobe interference was produced in the forming of the final correlation peaks.

The envelope function is then fed to a voltage comparator to produce pulses which undergo amplitude and width modifications for compatibility purposes, resulting in the reconstructed PCM signal QD. This representation lags the original PCM signal (Q) by 16 microseconds, which is a result of the delay created by the signal transition time in the surface wave devices.

In the receive processor, QD is used to generate a word pulse (WPD) whose trailing edge coincides with that of the last data pulse in a frame of QD. The voltage controlled oscillator in the processor produces a continuous stream of timing pulses (CPD) and every eighth of these pulses (CP8) is extracted and phase compared with WPD to obtain a constant phase difference, which achieves send/receive synchronization as shown in Figure 34. The waveform CPD then clocks QD through a shift register and the trailing edge of WPD performs the retrieval of the proper data frames for D/A conversion.

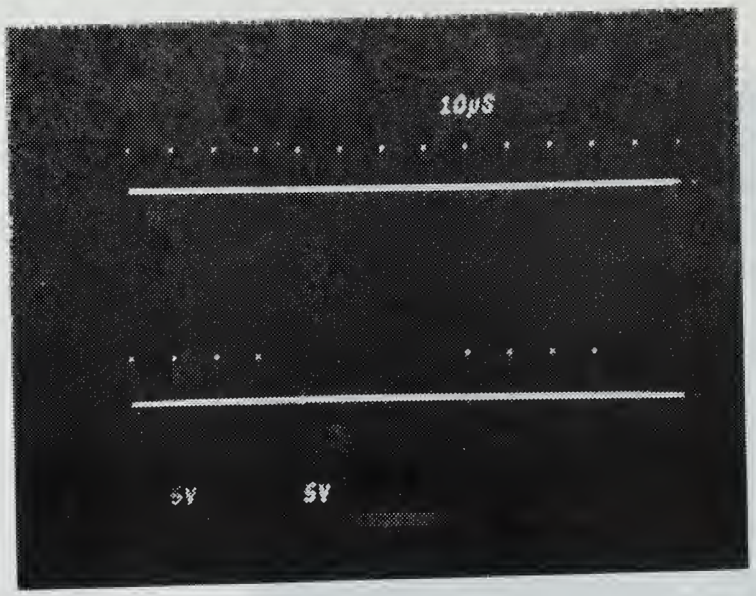

FIGURE 22

CLOCK, CP

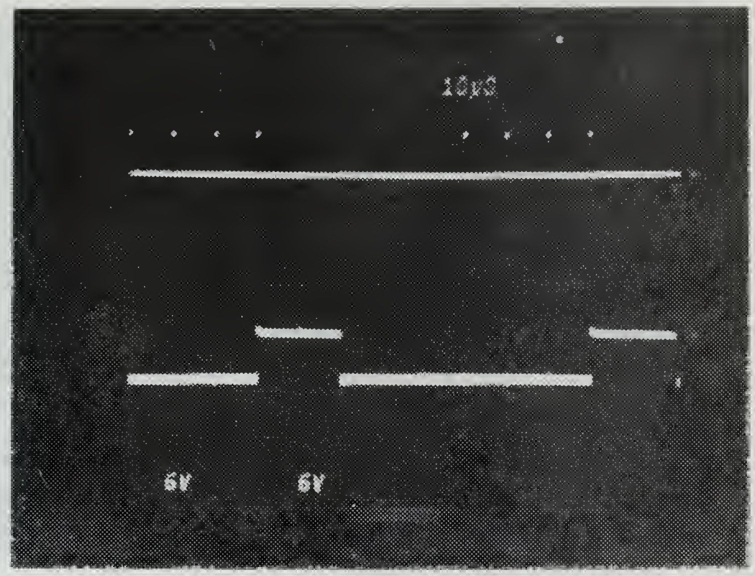

FIGURE 23

CP, CS

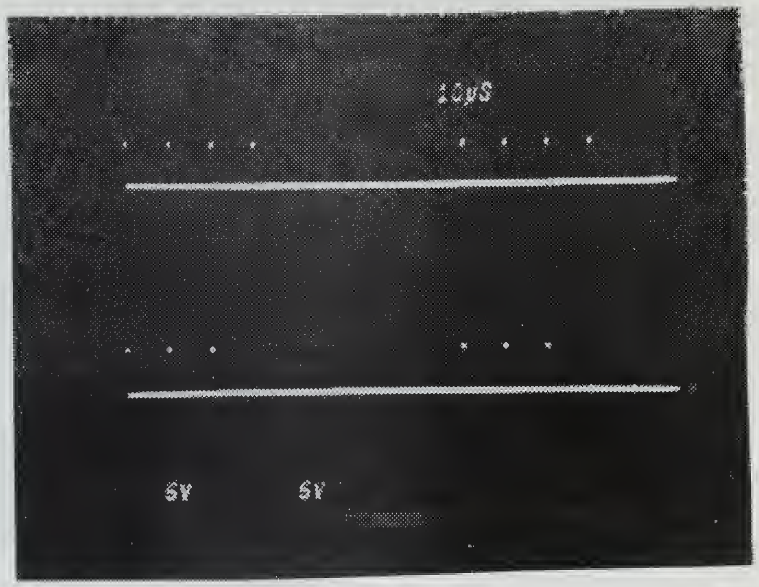

FIGURE 24

CP, Q

[illegible]

[illegible]

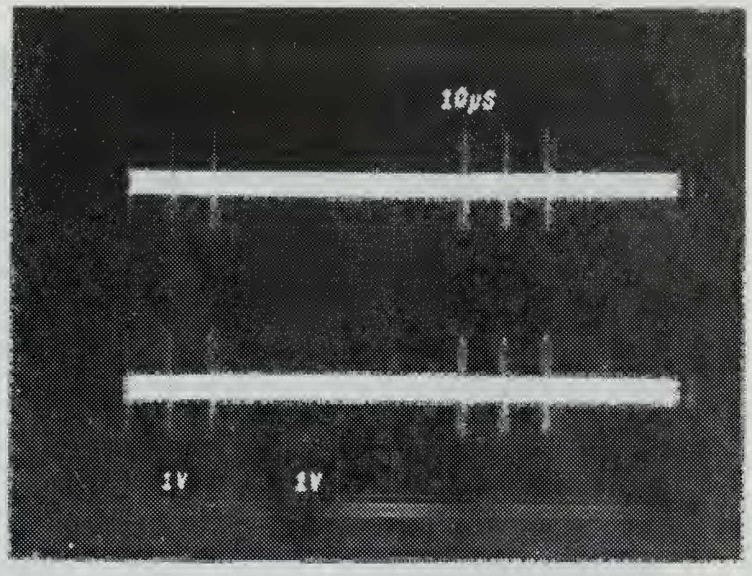

FIGURE 25

RF PULSES

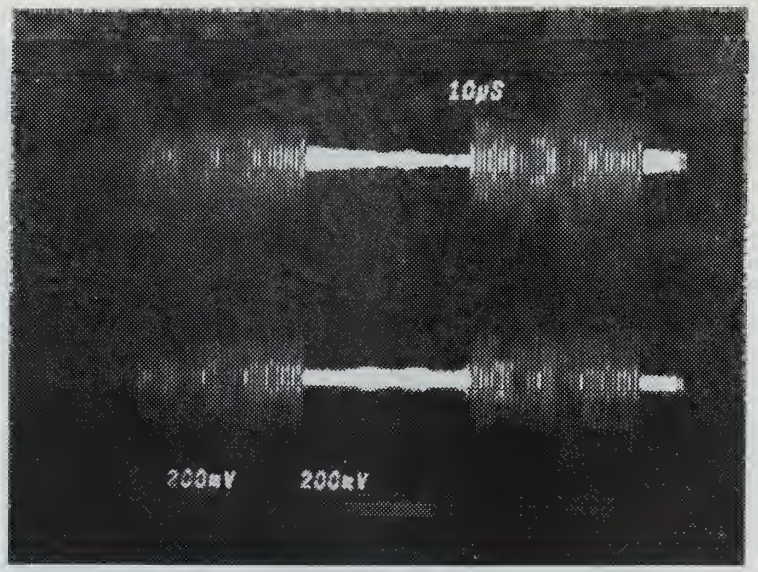

FIGURE 26

ASWDA, ASWDB

[illegible]

[illegible]

[illegible]

[illegible]

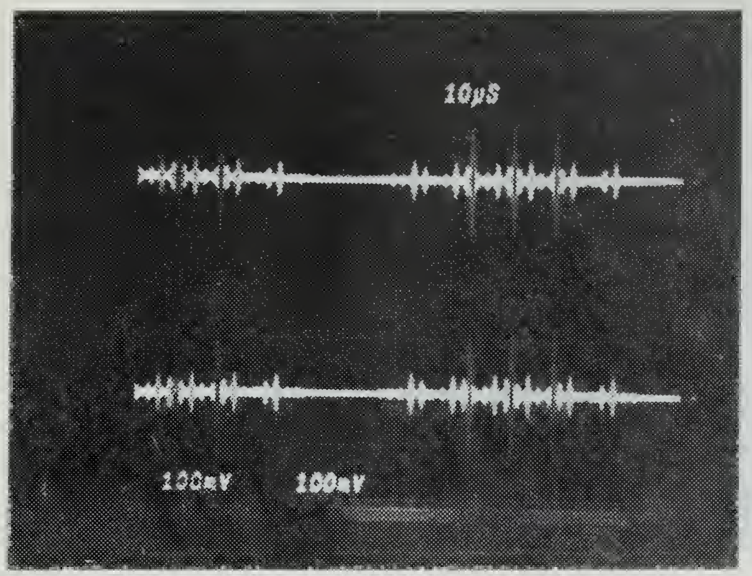

FIGURE 27

R_{AA}, R_{BB}

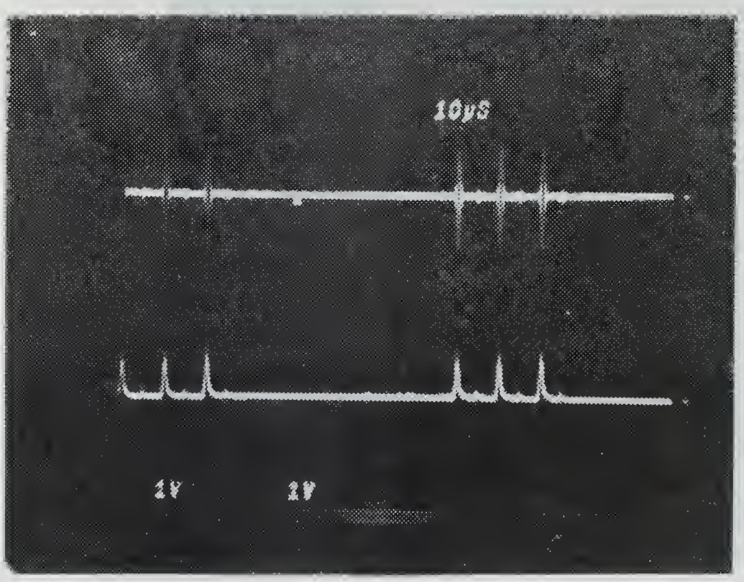

FIGURE 28

$R_{AA} + R_{BB}$, ENV

[illegible]

[illegible]

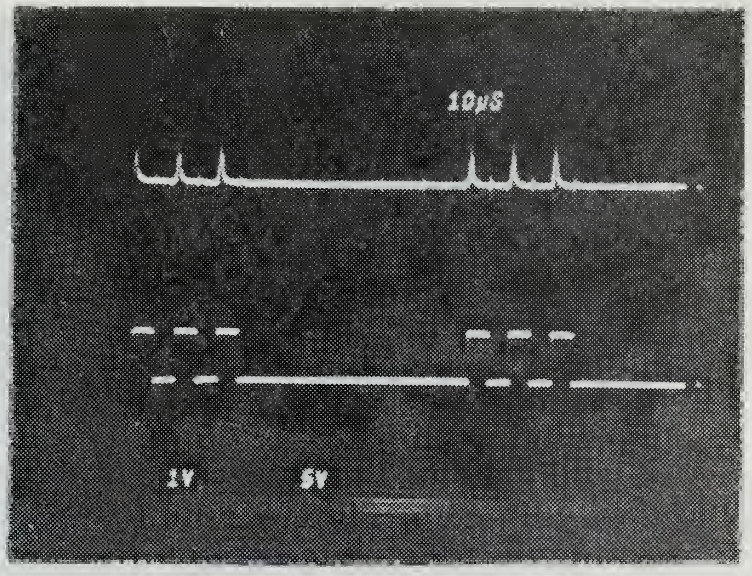

FIGURE 29

ENV, QD

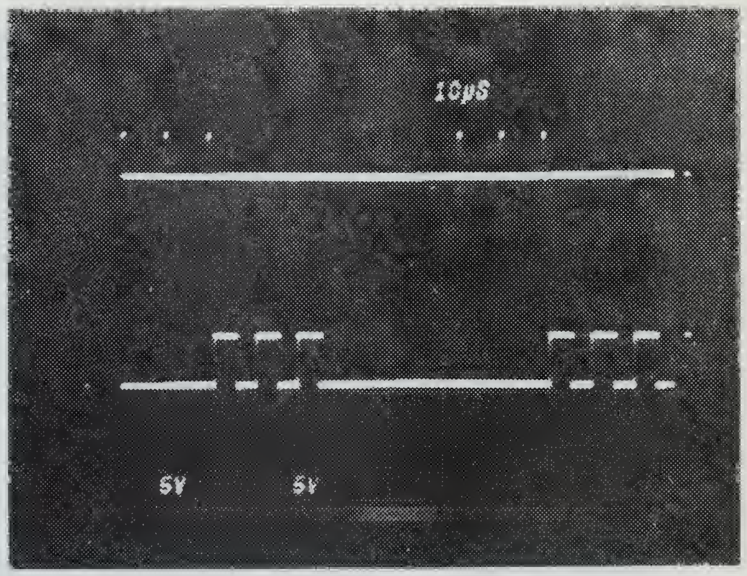

FIGURE 30

Q, QD

[illegible]

[illegible]

[illegible]

[illegible]

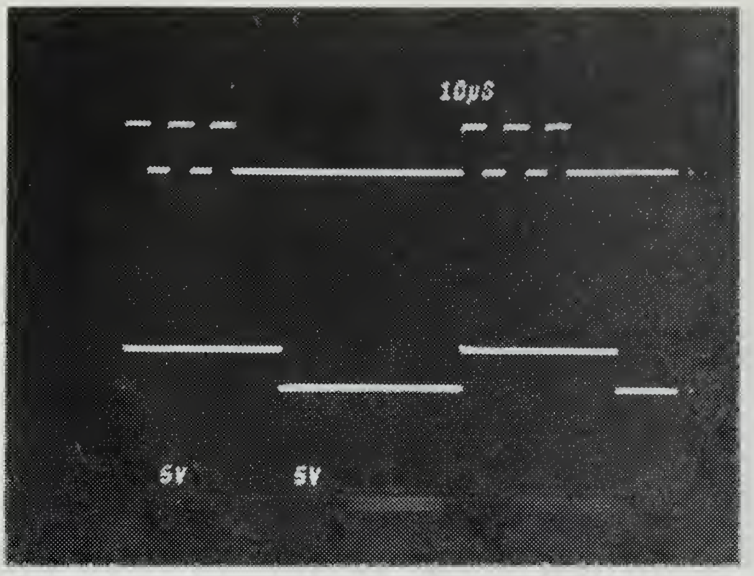

FIGURE 31

QD, WPD

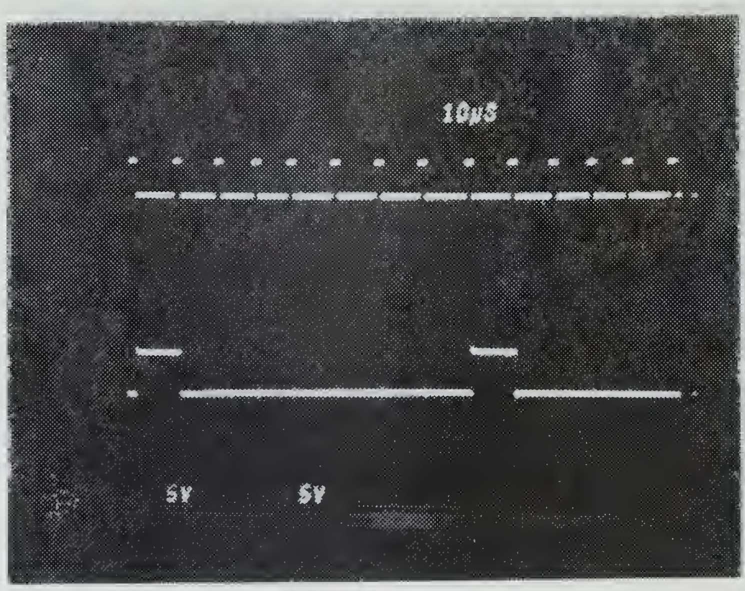

FIGURE 32

CPD, CP8

[illegible]

[illegible]

[illegible]

[illegible]

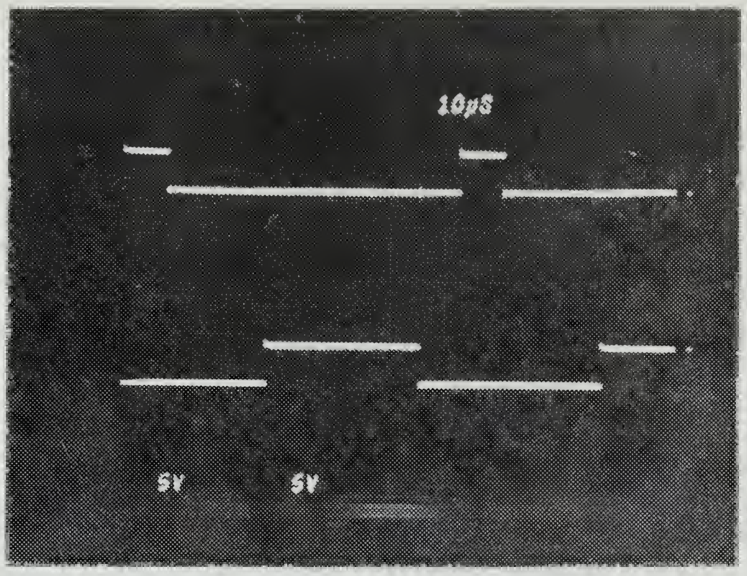

FIGURE 33

CP8, WPD

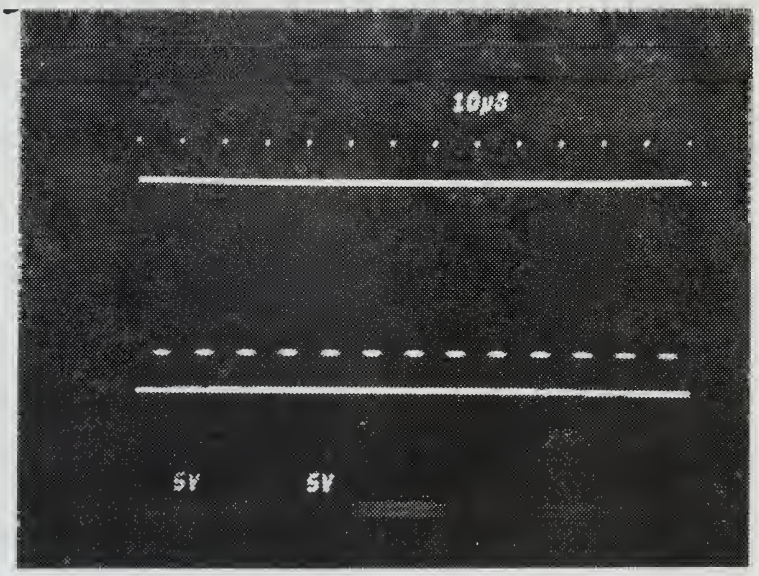

FIGURE 34

CLOCK, CPD

[illegible]

[illegible]

[illegible]

[illegible]

V. CONCLUSIONS

At the outset of this report, the statement was made to the effect that the finished product was to be a working model which would illustrate a technique whereby an audio signal could be processed into a form suitable for spread spectrum transmission, thereby giving the feature of covertness to a simple transceiver network. The actual MODEM developed does indeed fulfill these requirements, as has been illustrated in the preceding sections. The fact that it is a "toy" implies that in its completed state, the present system could not be used in an actual operational environment, but instead it realizes the theory required for the eventual design and construction of an actual transceiver.

In addition to fulfilling the requirements concerned with circuit design, reliability (realized by use of standard components) and simplicity, the added feature of a simple and efficient synchronization concept for a spread spectrum PCM system also evolved and was built into the circuitry. However, there are still many areas in which the MODEM could be expanded and improved upon to bring the solution of the original problem even closer to a completed state. Since the groundwork for an operating transceiver had been solidified by the realization of this MODEM, it was appropriate at this time to recommend topics of possible follow-on work which could be pursued toward the complete problem solution.

The first area of concern is the fact that the transmission in its present state is an on-off keyed (OOK) signal. A better method would be to employ a type of phase shift keying (PSK) where one phase of a carrier would represent the logical "high" state and a second phase would represent the logical "low" state. This would have the effect of having a continuous transmission on the air which would further reduce the possibility of detection of the signal by a non-intended receiver. Realization of this type of keying would of course require some type of phase synchronization between the send and receive processors, in addition to the timing synchronization already employed.

A second area of possible improvement is the method of detecting the correlation peaks as performed by the RF peak detector. The present method uses a voltage comparison to a predetermined threshold, a method which could possibly be ineffective in an exceptionally noisy environment. Instead, some type of signal-to-noise ratio detection could possibly be used so that the ability to detect the signal would not depend entirely on the present requirement that the peaks be at some fixed voltage amplitude.

The third consideration is of course design and fabrication of RF amplifiers of transmitter and receiver stages to make the device completely self-contained and therefore even closer to the final desired format - an actual transceiver. In this state actual on-the-air analysis of the transmitted signal could be performed, and possibly could result in the addition of further design modifications.

In any event, the initial task of demonstrating the signal processing technique has been realized, and it is the hope of the author that future research and development will eventually lead to a complete operational transceiver network.

APPENDIX A

ACOUSTIC SURFACE WAVE DEVICES AND GOLAY SEQUENCE SPECIFICS

Figure 35 shows a photograph of one of the ASWD's as it was connected in the circuit. The casing in which the device is mounted was milled out of a solid block of aluminum that measures 4 inches long by 2.2 inches wide by one inch thick. The top of the casing, seen in the photograph, was milled to allow sufficient space to mount the quartz substrate and to allow the inclusion of electrical feedthroughs from the external connection cavities on the reverse side of the

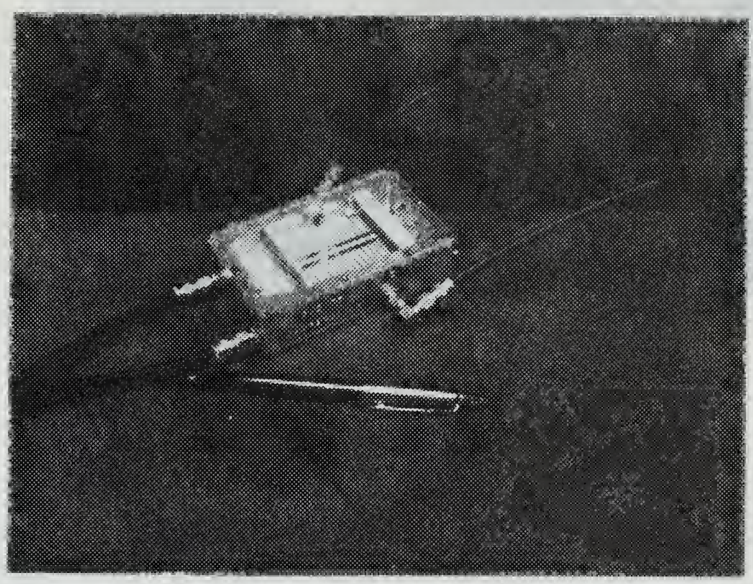

FIGURE 35

ASWD WITH EXTERNAL CONNECTIONS

[illegible]

[illegible]

[illegible]

[illegible]

casing, shown in Figure 36. There are six of these cavities, one for each of the three ports of each device, and each contains a transformer to obtain an impedence match between its respective feedthrough and a 50-ohm SMA external feedthrough connector, which allows coaxial cable connection to the device. These connectors can be seen in both Figures 35 and 36.

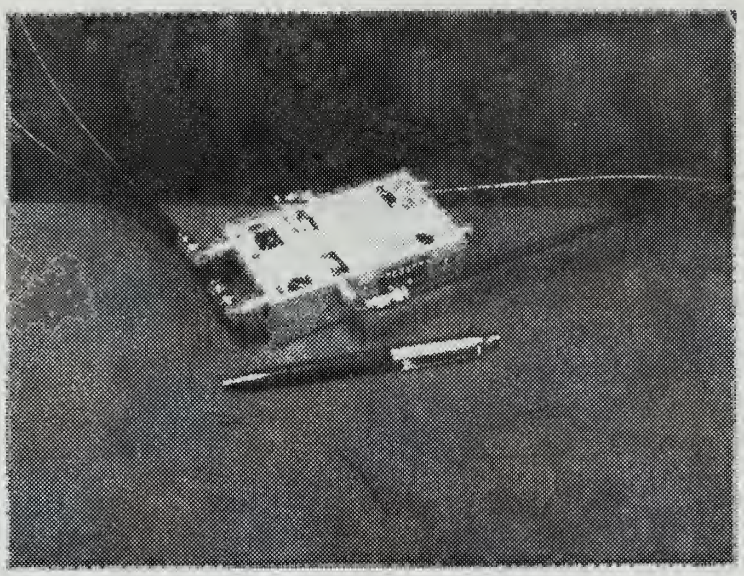

FIGURE 36

ASWD BOTTOM VIEW

The quartz substrate proper measures 3.0 inches by 1.5 inches by 0.1 inches and the 2000 Angstrom thick aluminum deposit occupies a total area of 2.6 inches by 1.5 inches. The deposited devices are composed of a single, ten-finger pair transducer at each end and sixteen phase coded ten-finger pair transducers in the center. This phase coding is the feature that actually implements the Golay sequences.

The relative phases of all transducers is shown in Figure 37. Using the technique outlined in Table 1 the autocorrelation functions of these codes could be obtained and the results would have major peaks of amplitude 16 with associated time sidelobes. The sum of these would then yield a major correlation peak of amplitude 32 with complete sidelobe cancelation.

ASWDA: 1 1 1 1 0 1 1 0 1 1 1 1 0 0 0 1 0 1
ASWDB: 0 0 1 0 0 0 1 1 1 0 1 0 0 1 0 0 0 0

FIGURE 37

ASWD TRANSDUCER PHASE CODING

This phenomenon was in fact produced by utilizing the impulse responses of the devices, which are depicted in Figure 38. This response was obtained by driving the devices with an electrical pulse of 30 nanosecond width. Each response is comprised of a sequence of 16 pulses of 21.4 megahertz frequency. Each pulse is one microsecond wide, giving the overall sequence a length of 16 microseconds. The shape of the individual pulses evolves from the convolution process on the substrate of 10-cycle rectangular surface waves with each of the 10 finger pair receive transducers, which yields individual pulses containing 20 cycles of the carrier frequency with a diamond shaped

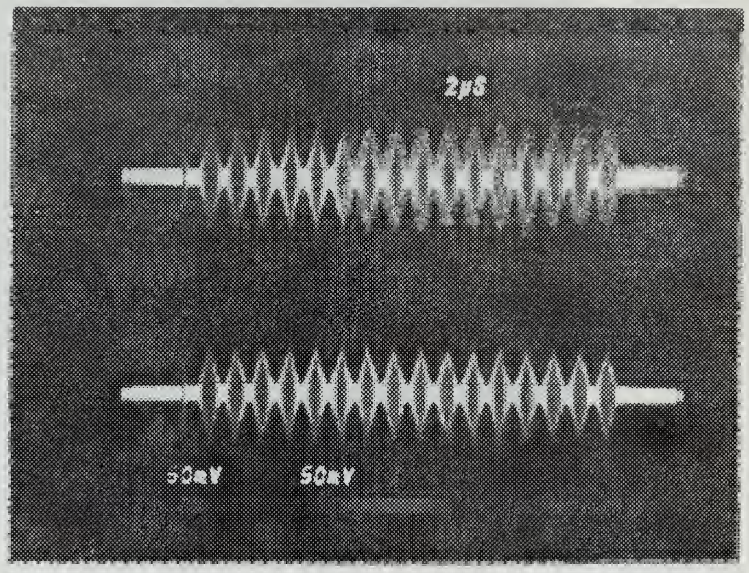

FIGURE 38

ASWD IMPULSE RESPONSE

envelope, as shown in the expanded view of Figure 39. Figure 40 illustrates the phase coding of the impulse responses by summing the waveforms of Figure 39. In this case the first pulses are in phase, and therefore additive, and the second pulses are out of phase and thus tend to cancel each other.

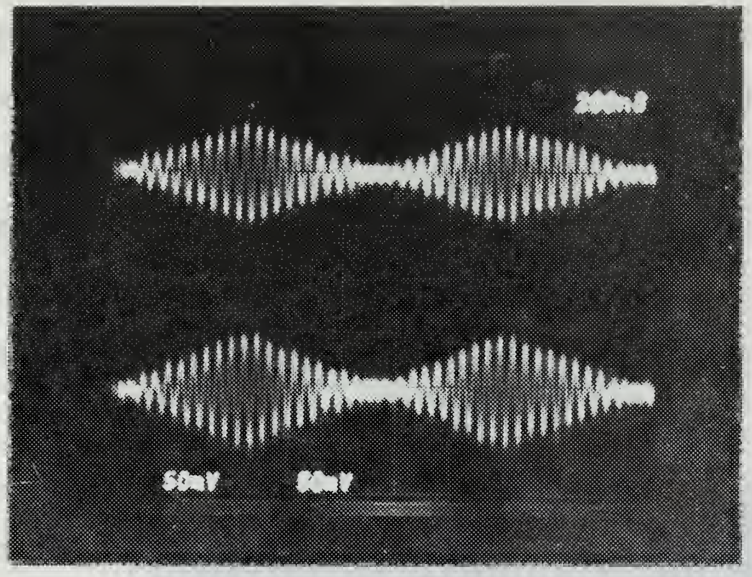

FIGURE 39

EXPANDED VIEW OF ASWD IMPULSE RESPONSE

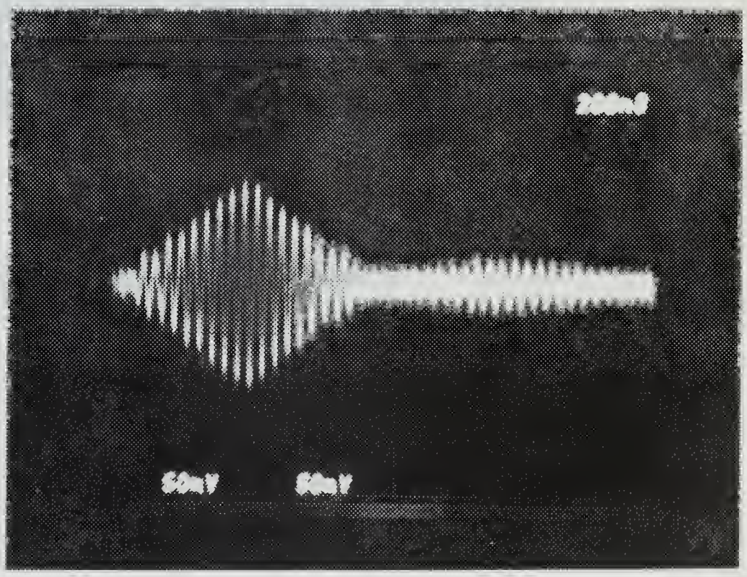

FIGURE 40

IMPULSE RESPONSE PHASE DIFFERENCES

[illegible]

[illegible]

[illegible]

[illegible]

The autocorrelation functions were then obtained by feeding the impulse responses to the appropriate matched devices and the results were as shown in Figure 41. These waveforms clearly depict the dominant center peaks and associated time sidelobes. The sum of these was then taken and the resultant center peak enhancement and sidelobe cancellation that resulted was as illustrated in Figure 42.

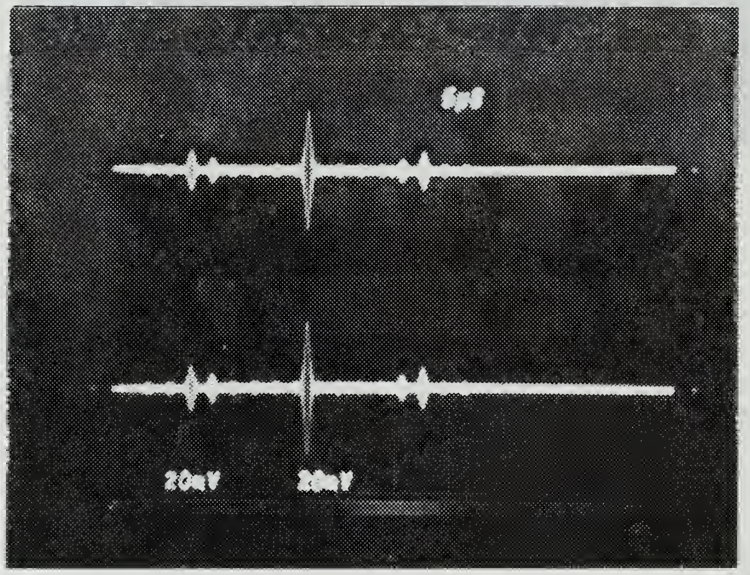

FIGURE 41

AUTOCORRELATION FUNCTIONS

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[illegible]

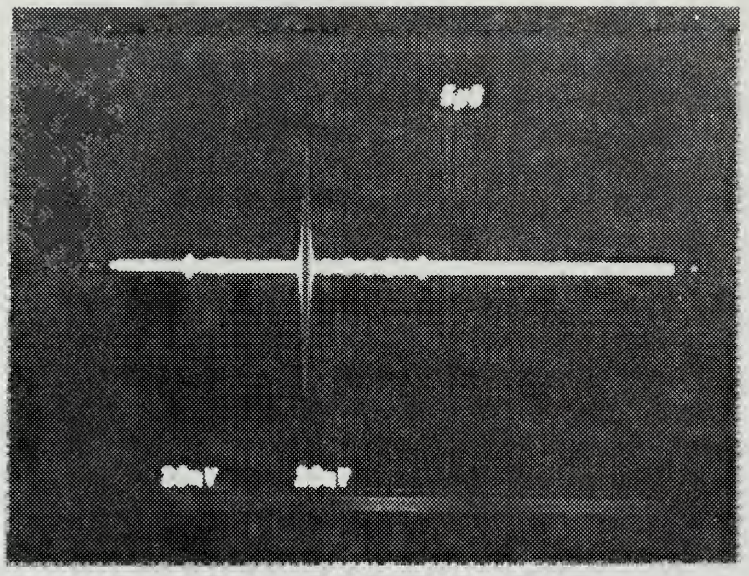

FIGURE 42

SUM OF AUTOCORRELATION FUNCTIONS

APPENDIX B

PCM SYNCHRONIZATION IN A SPREAD SPECTRUM APPLICATION

The concept presented here is concerned with synchronization of a pulse code modulated (PCM) system for use in a spread spectrum application. Specifically, the problem is that given a stream of digital data which represents a PCM signal, how does the receiver decide which groups of bits constitute individual data frames. The present method of accomplishing this involves periodic transmission of a coded bit group which is used by the receiver as a time reference from which the incoming bits are counted in increments of the known word-frame length to achieve proper data retrieval. This implies the necessity of complex pattern recognition hardware at the receiver and in the event of transmission error, a loss of a significant amount of data. In a spread spectrum system, this problem can be solved simply and efficiently, as described in the following paragraphs.

At the transmit side of a communications system, a signal is quantized and pulse code modulated to say, n bits. This implies that each data frame to be transmitted must contain at least these n bits. As previously stated, the specific problem at the receiver is one of deciding when a frame of data is present in order to successfully retrieve the transmitted data.

A block diagram of the transmitter timing is shown in Figure 43. A master clock is running at a fixed rate, with

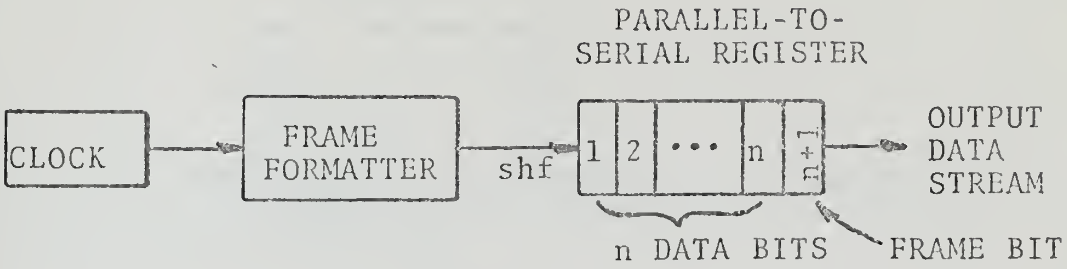

FIGURE 43

TRANSMITTER TIMING

pulse period T. This signal is modified by a "frame formatter" which selects an individual frame of length 2(n+1)T and allows clock pulses to occur only during the first (n+1) pulse periods of each frame, as shown in Figure 44. A data

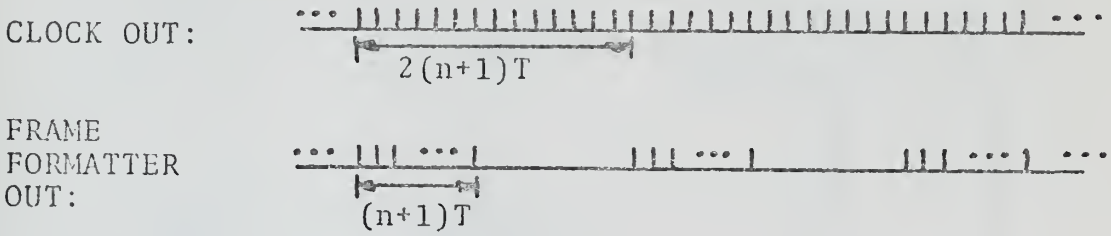

FIGURE 44

DATA FRAME FORMATTING

shift register, previously loaded with the n bits of data has its (n+1)th bit always loaded with a "1", or logical "high" state. When the data is shifted out of this register, a serial data stream will be created which adheres to the frame format described and will appear as shown in Figure 45. The first bit of each data frame is always "high"

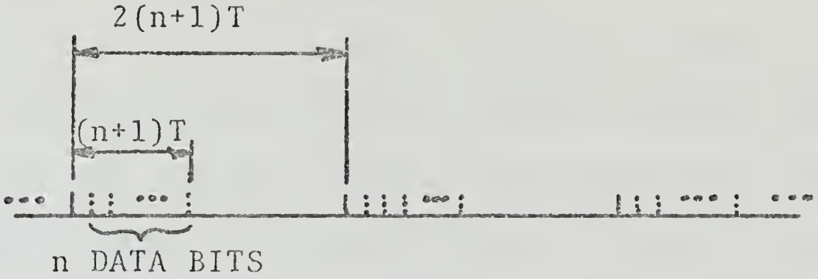

FIGURE 45

SERIAL DATA FORMAT

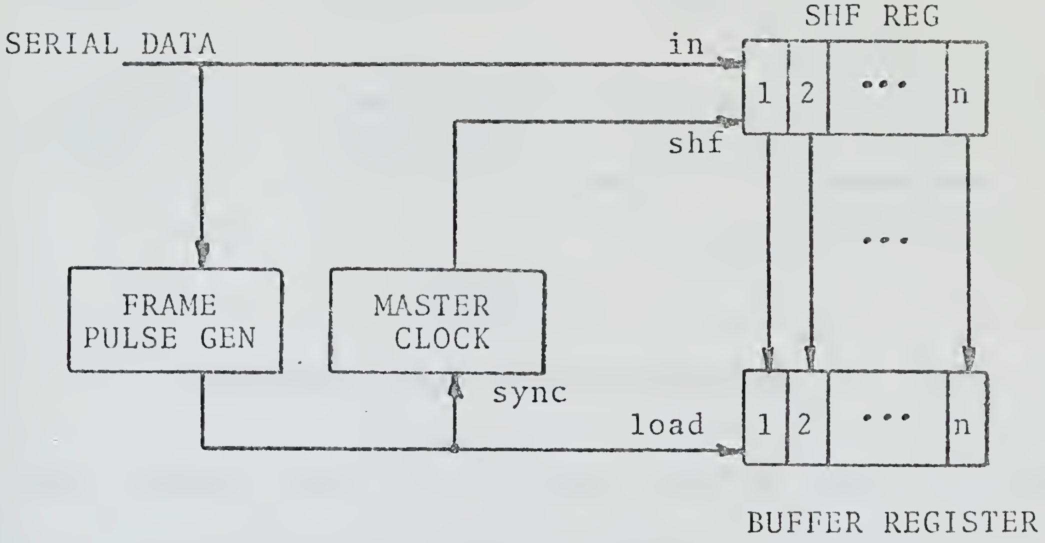

FIGURE 46

RECEIVER TIMING

followed immediately by n bits of data, which in turn are followed by (n+1) logical "zeroes."

A block diagram of the receiver timing is shown in Figure 46. The incoming signal is fed to a serial input shift register and also to a frame pulse generator which, when triggered produces an output pulse of width T_f, where

$$nT < T_f < (n+1)T.$$

In other words, the trailing edge of this pulse occurs during the last of the data pulses, which occupies the (n+1)th slot of the data frame, as shown in Figure 47.

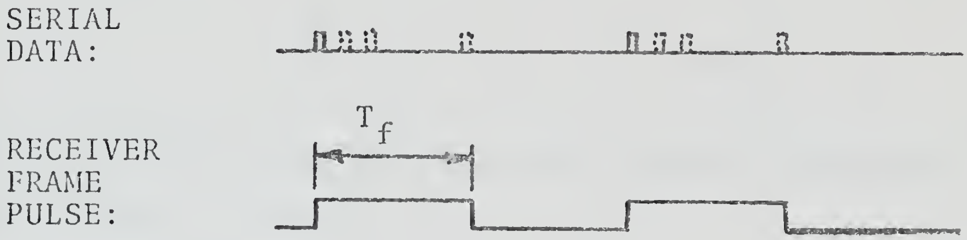

FIGURE 47

RECEIVER FRAME PULSE GENERATION

The leading edge of this frame pulse is used to synchronize the receiver master clock, which is designed to synchronize on every 2(n+1)th of its pulses. The output of the clock is used to pulse the input shift register, which causes the incoming data to be serially entered into the register. Assuming that the frame pulse is in fact generated by the first bit of the incoming frame, the trailing

edge is now used to trigger parallel loading of the buffer register at precisely the time that the n bits of data are present in the shift register.

If, because of a transmission error or a system malfunction the first bit of a data frame is not set, the receiver frame pulse will then be generated by the next available "high" pulse, thus causing loss of synchronization. For analysis of this problem, consider the "worst case" example, that is the frame pulse is generated by the last data pulse, which is in position (n+1)T in the data frame. Since it has been specified that the pulse width of the frame pulse satisfied

$$nT < T_f < (n+1)T$$

then the trailing edge of this particular frame pulse will occur at time t, where

$$(2n+1)T < t < 2(n+1)T$$

which simply states that it will not overlap the first bit of the next incoming frame. Thus, the next data frame will resynchronize the system, resulting in loss of synchronization for only one data frame. Therefore the PCM data is successfully retrieved at the receiver with a minimum loss of information.

An apparent disadvantage of this synchronization method is that for one half of the time, no data is transmitted, implying that data would have to be transmitted at a double

rate of a normal PCM system, thus resulting in a larger bandwidth requirement. However, it was stipulated that this concept is intended for use in a spread spectrum system, where bandwidth spreading is the prime criterion. The synchronization scheme then readily lends itself to such a system since it actually enhances the spreading process, and provides the additional advantage of minimizing data loss.

APPENDIX C

SEND AND RECEIVE PROCESSOR DETAILS

The schematic wiring diagram of the send processor is depicted in Figure 48. All component pin connections are labelled by pin numbers and all resistor values shown are in ohms. A functional description of each "module" is given in the following narrative.

The "Audio Preamplifier" consists of a type N5558V "Dual Operational Amplifier" integrated circuit. Its function in this application is to accept an audio signal from a microphone and amplify this signal to the full scale input range of the A/D converter (+/- 5 volts), which was accomplished by connecting the two operational amplifiers in series. The first amplifier stage has variable voltage gain ranging from 0 to 1000, and the second stage has a fixed gain of 10.

The A/D converter is a ZELTEX model ZD470 8-bit converter. Its purpose is to digitize samples of the audio preamplifier output upon command from the timing circuitry. Only the three most significant bits of the binary result are used in this circuit, and these are presented in parallel format to the "Output Shift Register."

This register is a type TTL 7495 4-bit multipurpose register, and it performs the primary function of parallel-to-serial data format conversion. In its loaded state, the

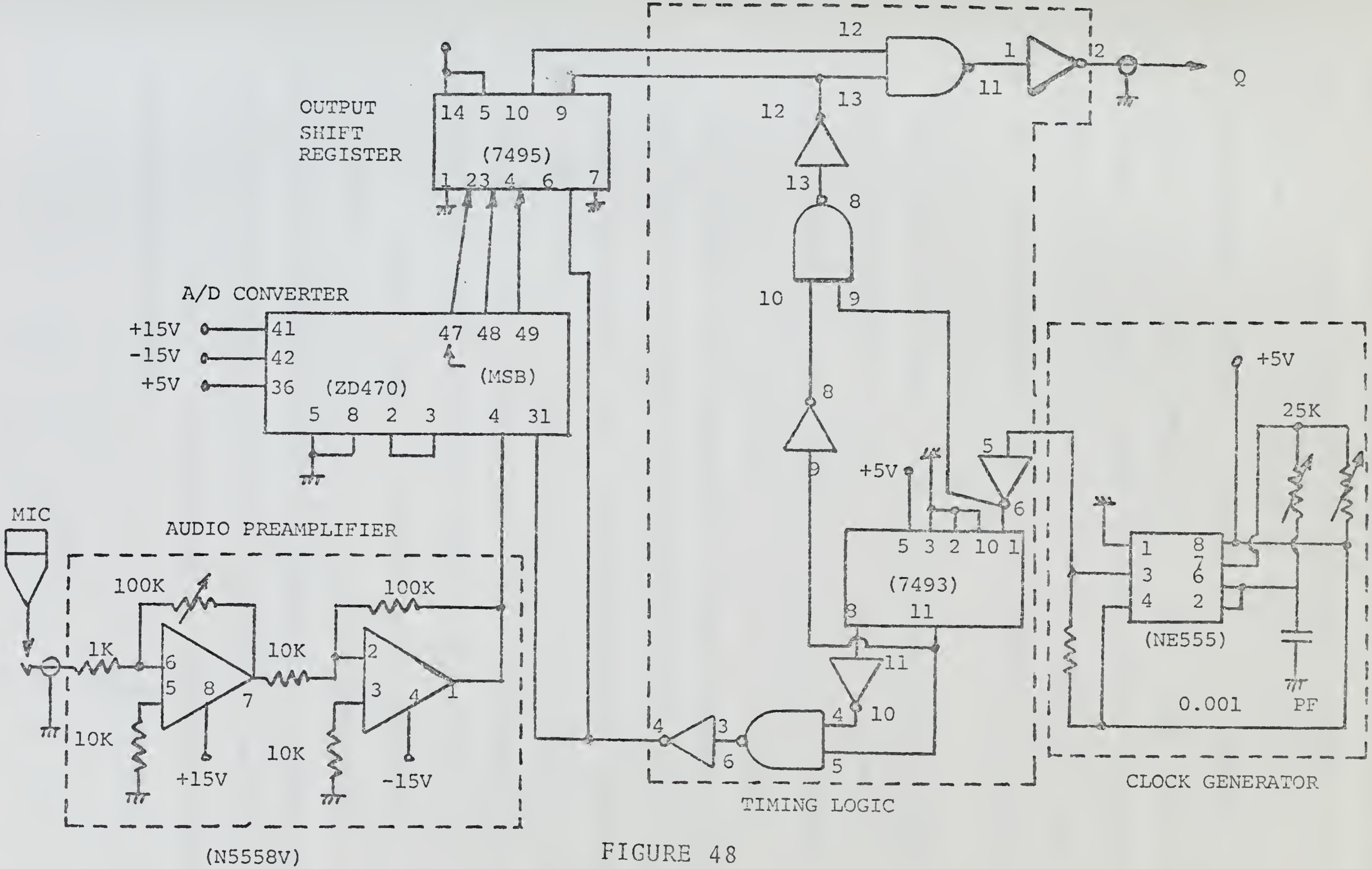

FIGURE 48

SEND PROCESSOR SCHEMATIC WIRING DIAGRAM

register contains a frame of data in the following format: bit 1: most significant bit of the audio sample, bit 2: second most significant data bit, bit 3: third most significant data bit and bit 4: always set to a logical "high", as shown by the pin 5 connection. This "high" bit serves as the "frame bit" which is used by the timing circuitry in the receive processor to achieve circuit synchronization. The data is shifted serially out of this register in the proper format by the timing waveform CP.

The "CLOCK Generator" consists of a single integrated circuit of type NE555 "Timer." Its primary function is to produce the master clock waveform CLOCK with variable parameters of pulse width and pulse repetition frequency.

The "Timing Logic" consists of three digital integrated circuits: (1) a TTL 7493 4-bit binary counter, (2) a TTL 7404 hex inverter and (3) a TTL 7400 quad two-input NAND gate. The 7493 is a ripple counter and is used as a three bit counter in this application. THe IC is pulsed by CLOCK, producing the output sequence shown in Figure 49. Note that a three bit binary count is periodic over eight pulse periods, which is the overall length of the data frames used in the MODEM. This sequence used by the remainder of the logic circuitry to generate the timing waveform CP and the convert start pulse CS, which, using the logic variables shown in Figure 49, are defined by the following logic equations:

$$CP = (X1') \cdot (CLOCK)$$

$$CS = (X1) \cdot (X2')$$

X1	X2	X3	
0	0	0	CP
0	0	1	
0	1	0	
0	1	1	
1	0	0	CS
1	0	1	
1	1	0	
1	1	1	
0	0	0	(Periodic)

FIGURE 49

BINARY COUNTER OUTPUT STATES

where a primed (') variable designates the logical complement of that variable. These equations merely state that CP will be a sequence of four pulses occuring during the first half of each frame of eight pulses and CS will be a logical level that is "high" during the fifth and sixth pulse periods of each frame. This is illustrated by the labelling in Figure 49.

The format of CP is such that the data frame format adheres to that required by the synchronization concept and CS occurs such that data samples will be taken, digitized and passed to the output shift register during the latter half of each preceding frame.

Figure 50 shows a schematic wiring diagram of the digital portion of the receive processor and Figure 51 shows the

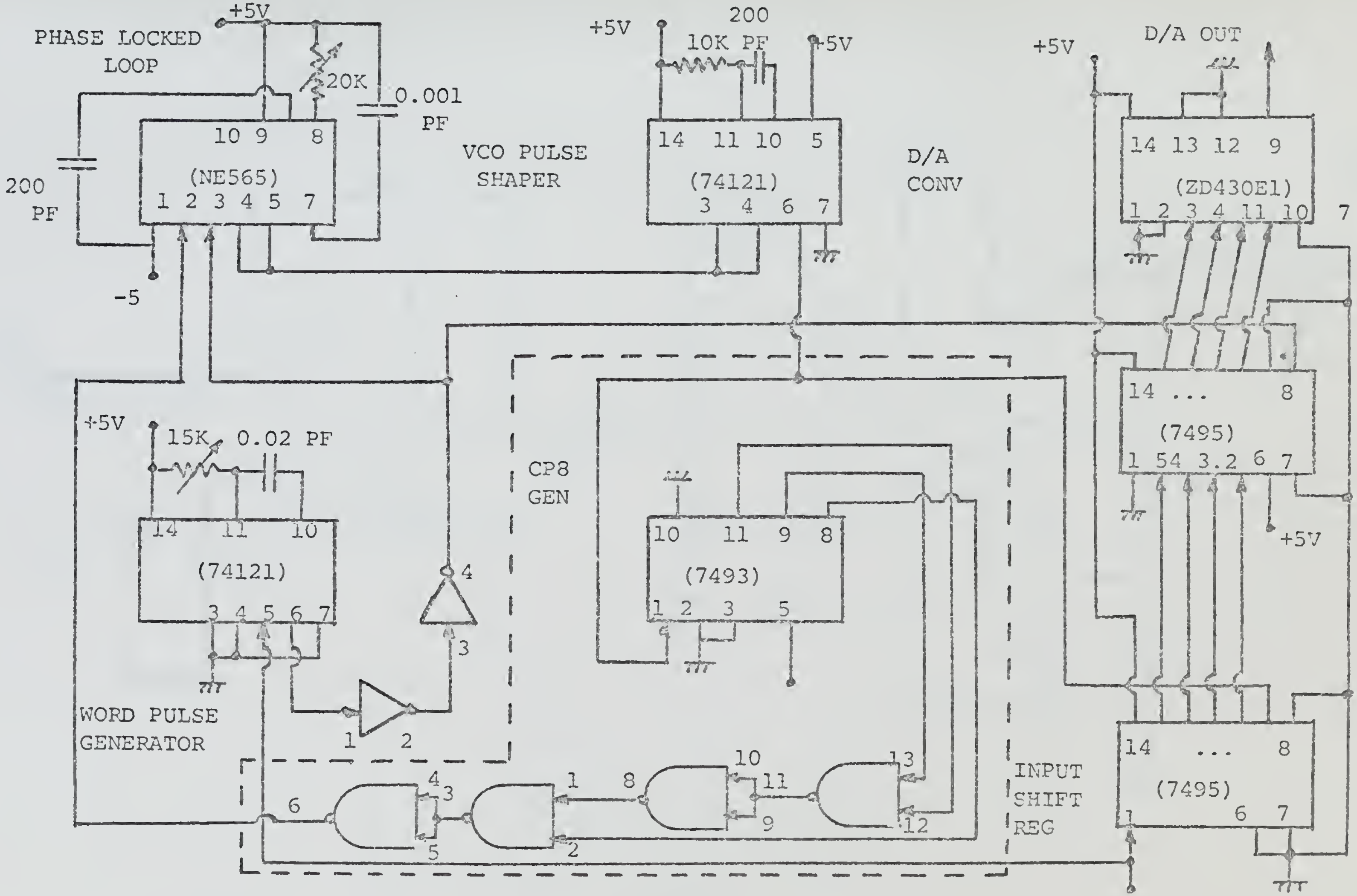

FIGURE 50

RECEIVE PROCESSOR DIGITAL SCHEMATIC WIRING DIAGRAM

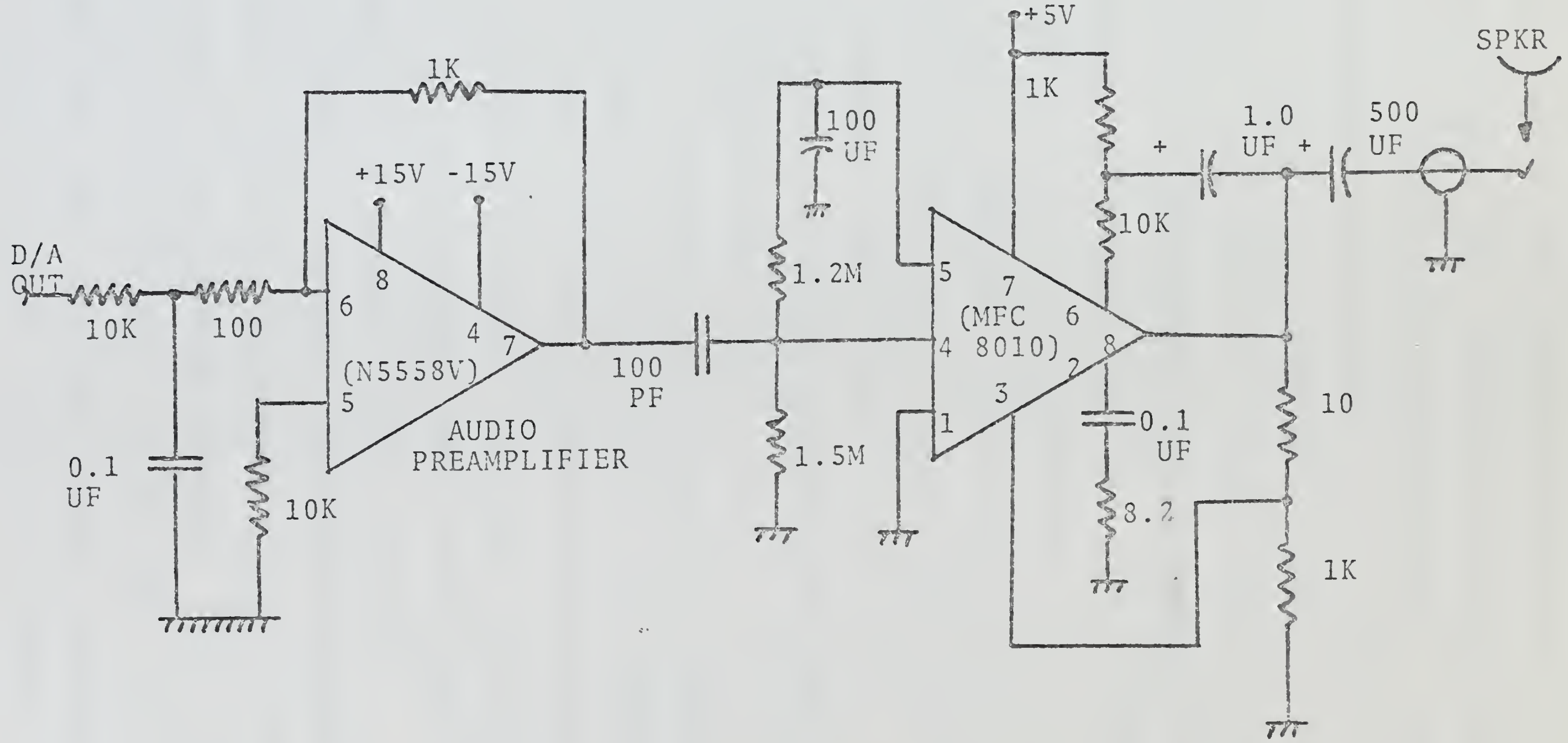

FIGURE 51

RECEIVE PROCESSOR ANALOG SCHEMATIC WIRING DIAGRAM

schematic for the analog, or audio portion. The following paragraphs describe the components illustrated.

Refer to Figure 50. The input data stream, QD is fed simultaneously to the "Input Shift Register", a type TTL 7495 multipurpose 4-bit register, and the "Word Pulse (WPD) Generator". The latter component is simply a one-shot multivibrator, type TTL 74121, whose output is triggered by the occurrence of the leading edge of an input pulse. The output pulse is of variable width, so the trailing edge of WPD can be set to any desired position.

The "Phase Locked Loop" (PLL), type NE565 has its VCO free running frequency set at a value approximately equal to that of the master clock in the send processor. This is done so that in the case of synchronization loss, the frequency differences will not be so great that the capture range of the PLL is exceeded, therby precluding re-phasing of the VCO. The output of the VCO is fed to the "VCO Pulse Shaper" which is another TTL 74121 one-shot multivibrator, which acts as a pulse width control for these timing pulses. The output of this multivibrator is the actual timing sequence (CPD) used in the remainder of the circuitry.

CPD is used to clock the "Input Shift Register" and is also used to drive the "CP8 Generator" which extracts every eighth pulse of the incoming sequence. This is done through the use of a TTL 7493 binary counter and a TTL 7400 quad two-input NAND gate. The binary counter produces the same output sequence depicted in Figure 49, and the output of the

entire logic set satisfies the logic equation

$$CP8 = (X1)\cdot(X2)\cdot(X3).$$

This pulse is then fed to one input of the phase comparator inputs of the PLL, the other comparator input being driven by WPD. This is the stage at which the synchronization concept described in Appendix B actually begins.

Once synchronization is obtained, the incoming data is then shifted through the "Input Shift Register", and the trailing edge of WPD is used to clock the parallel outputs of this register into the "Buffer Register", which is a type TTL 7495 multipurpose 4-bit register used in a negative edge-triggered parallel input mode. This register then holds the data at the inputs of the "D/A Converter" a ZELTEX model ZD430E1, which converts the binary representations into an analog form.

Referring now to Figure 51, the analog output of the D/A converter is fed through a simple low-pass resistor-capacitor filter, to the "Audio Preamplifier", which consists of a type N5558V operational amplifier. The low-pass filter smoothes out the D/A converter output prior to amplification by the audio stages. The output of the preamplifier is then fed to the final stage, which is a MFC 8010 "Audio Power Amplifier". This stage is used to develop the power necessary to drive an external speaker, which is the final stage of processing in the system.

APPENDIX D

DETAILS OF THE INTERFACE ELEMENTS

The schematic wiring diagram of the RF pulse generator is shown in Figure 52. The following discussion refers to the description of the components in that diagram.

The data stream generated by the send processor (Q) is fed to a MC 1545 "TTL Switched Analog Gate" to perform the actual switching function in that component. The signal input to the gate is provided by a crystal controlled free running oscillator whose center frequency is 21.35 megahertz. The oscillator consists primarily of a CA 3028 differential amplifier wired in the oscillation mode.

The output of the analog gate then consists of pulses of the 21.35 megahertz frequency, the width of which are determined by the pulses contained in Q, and this waveform is then fed to a "power splitter", which is a MERRIMAC PD-20-300, MOD 2. The resultant output is then two identical channels of pulsed RF, which can be used to drive the Golay complementary coded ASWD's.

Figure 53 depicts the schematic wiring diagram of the correlation peak detector. The incoming correlation peak waveforms, which result from the summation of the individual autocorrelation functions produced by the receive ASWD, are fed through a type 1N277 diode which performs the function of extracting the envelope of the incoming signal.

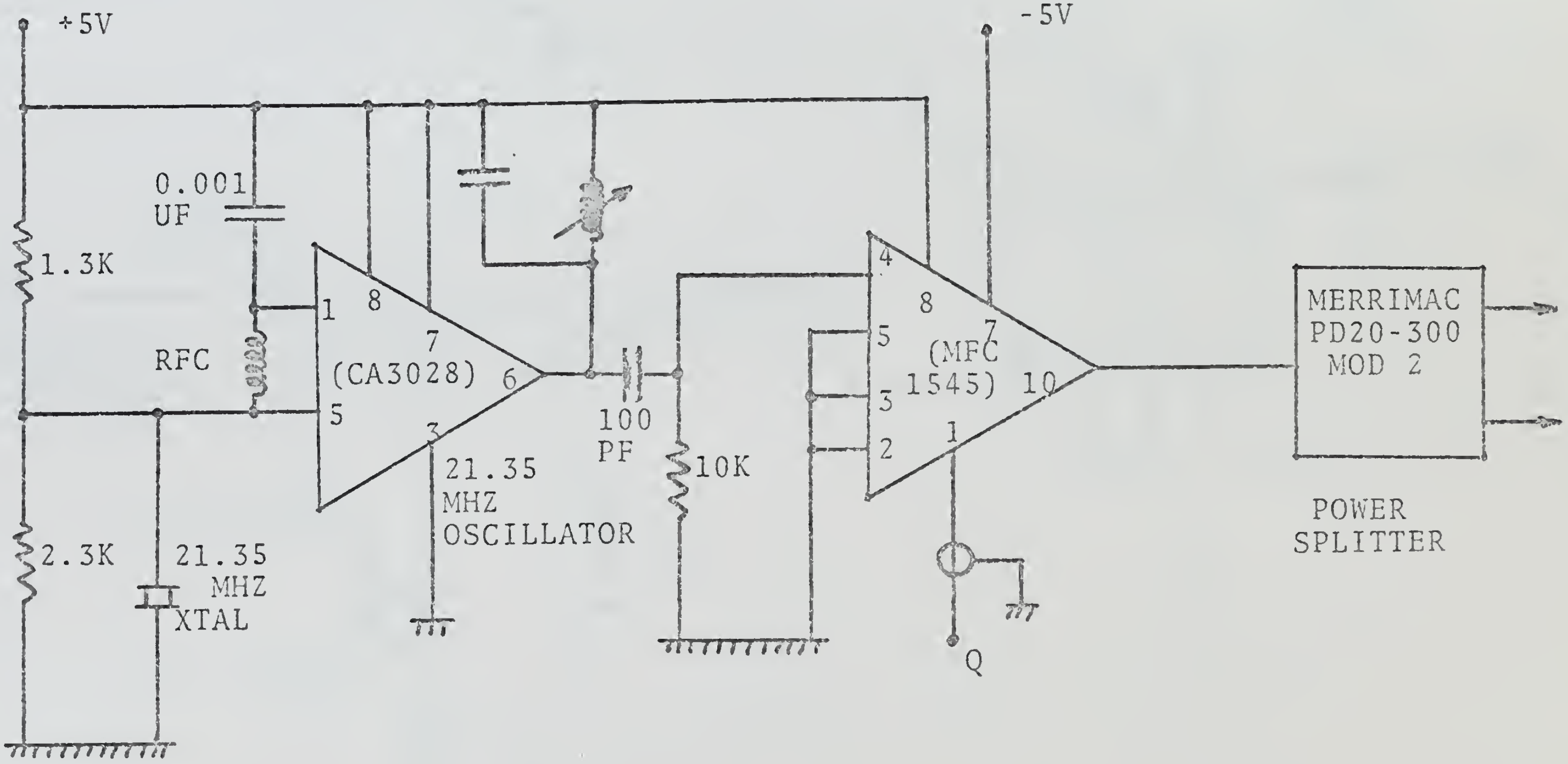

FIGURE 52

RF PULSE GENERATOR SCHEMATIC WIRING DIAGRAM

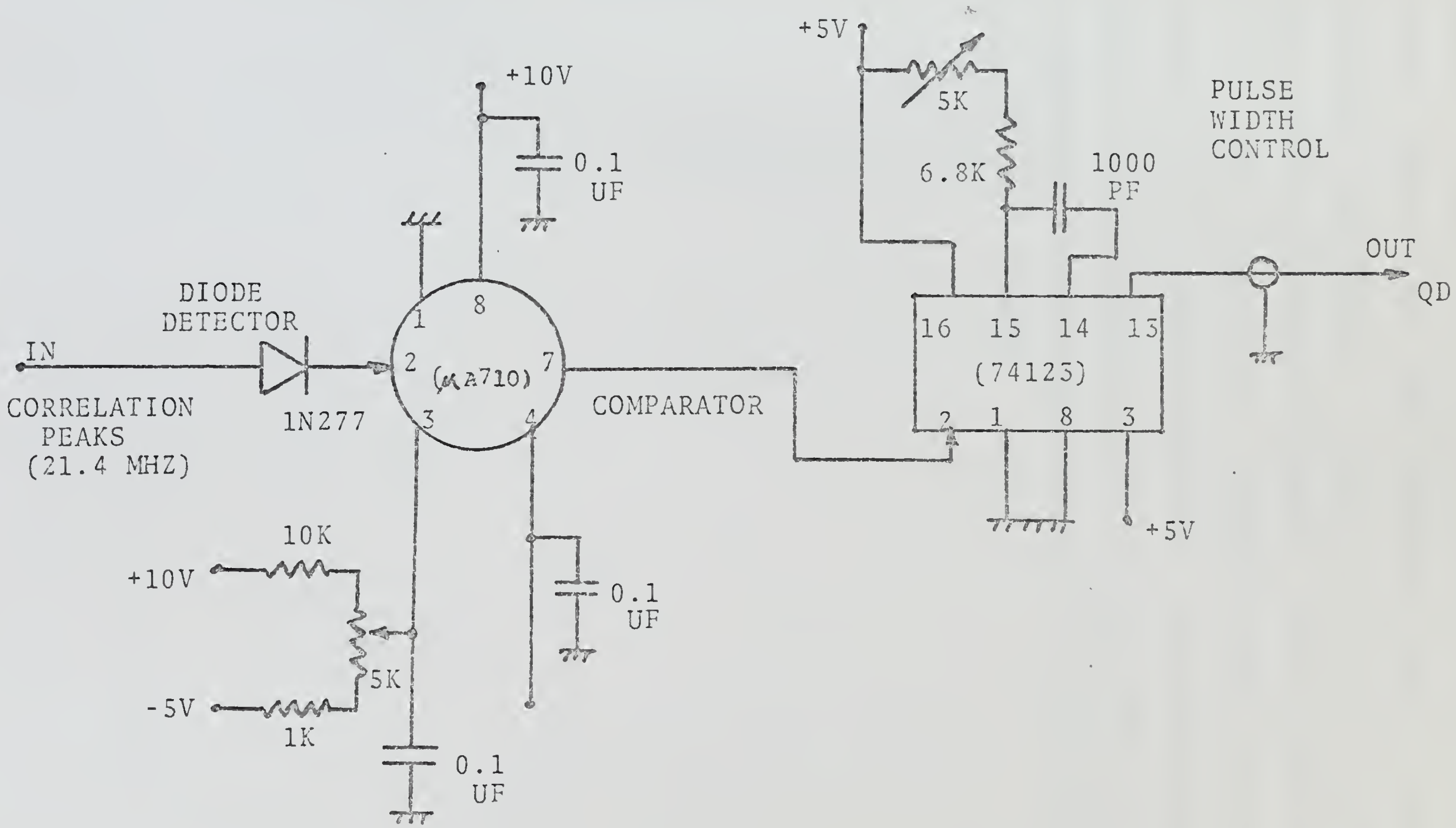

FIGURE 53

PEAK DETECTOR SCHEMATIC WIRING DIAGRAM

This envelope is then fed to a μA710 Comparator, which produces an output pulse of fixed width (equal to 6 microseconds) whenever the input waveform crosses a predetermined threshold. These pulses are then modified in amplitude and width by a TTL 74123 multivibrator, which produces the resultant output sequence QD, compatible with the logic circuitry in the receive processor. The multivibrator also adds the feature of pulse width control, which was necessary to compensate for an occasional drift in the receive processor timing frequency.

APPENDIX E

OVERALL SYSTEM AND POWER SUPPLY DETAILS

To alleviate the problem of supplying the various DC voltages to the active units of the MODEM from separate power supplies, a single supply source was fabricated, the schematic wiring diagram of which is depicted in Figure 54. The "heart" of the supply is comprised of two ZELTEX modular power units, models ZP5500 and ZM15200, which are capable of delivering 5 volts DC at 500 milliamperes and 15 volts DC at 200 milliamperes respectively. As shown in Figure 54, the outputs of these modules were fed to a network of zener diode and resistor combinations to derive the individual voltages required by each active device. The actual distribution was based on the power budget of each device and the capabilities of the two power modules.

In its final format, the MODEM was physically packaged into functional modules which were interconnected by RG-58 coaxial cable. With the exception of the surface wave devices, which were equipped with SMA type connectors, all cable connections were of BNC type. The microphone and speaker plugs consisted of simple telephone type jacks.

Two additional features included in the packaging of the MODEM consisted of external test point connections and external adjustment of variable parameters. In the send processor, the test points were taken from CLOCK and CP to

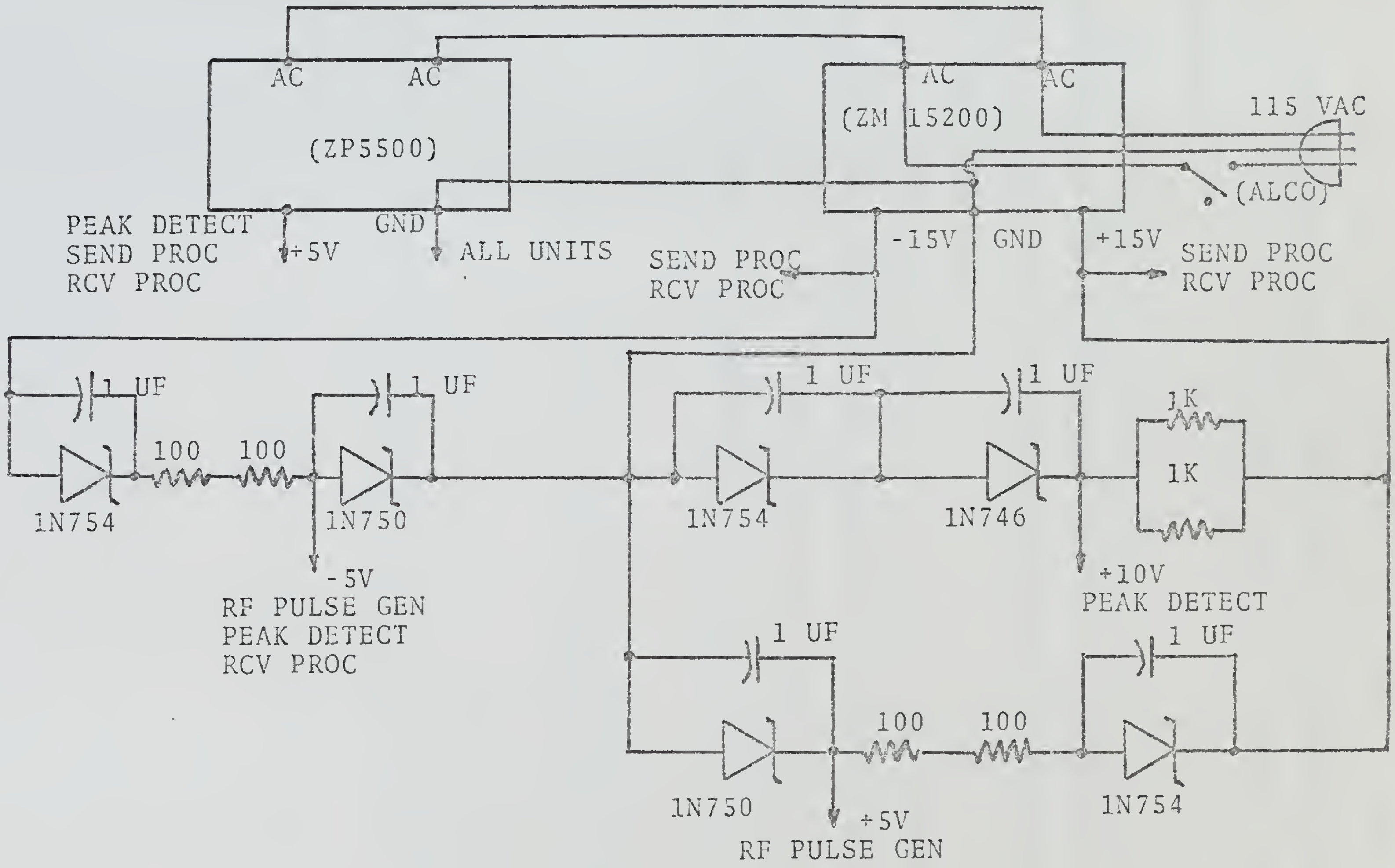

FIGURE 54

SYSTEM POWER SUPPLY SCHEMATIC WIRING DIAGRAM

facilitate trouble shooting of the timing circuitry. The parameters that can be externally adjusted in this device are the pulse width and repetition frequency of CLOCK.

In the RF peak detector unit, the external adjustments of QD pulse width and comparator threshold voltage are provided.

The final unit, the receive processor, has test point connections to CPD and WPD, and external adjustments of WPD pulse width and the free running frequency of the voltage controlled oscillator.

The overall combination of test points and external adjustment ports provide the capability of maintaining the working status of the MODEM without the necessity of gaining internal access to the modules.

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MODEM

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A practical solution to the problem of realizing a signal processing method for a covert voice communications system was the objective of the thesis. Spread spectrum technology in the form of Golay complementary sequences implemented with acoustic surface wave devices was utilized to achieve this processing.

The resultant device was an audio transceiver MODEM in which a specially coded form of pulse code modulation (PCM) was applied to a voice signal to enable application of the spread spectrum concept. The technique exploited spread the 3 KHZ voice modulation over a one MHZ bandwidth. A method of PCM synchronization evolved which achieves system send/receive synchronization with a minimum of data loss and a minimum amount of actual hardware.

Highly involved theoretical analysis was de-emphasized in the thesis in order that engineering requirements could be satisfied in the working device that resulted.

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